VERY HIGH SPEED INTEGRATED CIRCUITS

-VHSIC-

ANNUAL REPORT FOR 1986

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VHSIC PROGRAM OFFICE

OFFICE OF THE UNDER SECRETARY OF DEFENSE FOR ACQUISITION

31 December 1986

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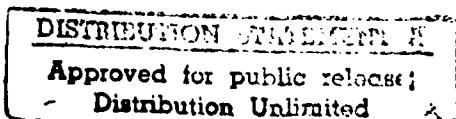
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FOREWORD

The VHSIC Program is in its sixth year in the development of advanced integrated circuits for military systems. The goals of the program have remained essentially the same as those set when the program was started. If anything they have become even more sharply focused on getting VHSIC technology as quickly, as economically, and as effectively as possible into fielded system use.

During 1986, a number of significant milestones were passed. Phase 1 of the program, involving the development and demonstration of 1.25 micron chip technology, has been completed. The effort has now turned to getting the 1.25 micron chips on the Qualified Products List for use by acquisition managers and to the development of the submicron generation of silicon integrated circuits in Phase 2. The use of VHSIC chips and their performance advantages have been demonstrated in operational systems such as the AN/ALQ-131 airborne electronic warfare pod and the AN/UYS-1 airborne anti-submarine warfare sonobuoy equipment. Even wider applications of VHSIC technology are taking place in developmental systems such as the Enhanced Position and Location System for ground troop use.

This report describes the VHSIC program, its origin, its goals, its accomplishments, and its status. Since this is the first report of the program for general distribution, the major VHSIC efforts are summarized from the beginning of the program. Subsequent annual reports will focus primarily on the highlights of the previous year.

VHSIC has been, and remains, one of the significant programs of the Department of Defense. It is an investment of DoD management and funding resources in the electronic technology needed to maintain a superior arsenal of weapons for the defense of the United States. The VHSIC program office is dedicated not only to developing this technology but also to making it a widely available industrial capability for the production of military electronic systems.
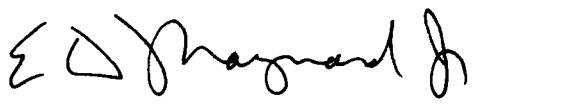
E. D. Maynard, Jr.
Director
Computer and Electronics Technology

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EXECUTIVE SUMMARY

1986 HIGHLIGHTS

During calendar year 1986, very substantial progress was made in the VHSIC program. The most significant milestone was the completion of the Phase 1 development of 1.25 micron[1] technology.

The 1.25 micron IC chips are now being qualified to JAN specifications so that they can be placed on the DoD Qualified Products list (QPL). These steps follow the first demonstrations of VHSIC in operational systems and represent the transition of the technology from the developmental stage into the U.S. semiconductor industrial base. A growing list of technology insertion programs provides evidence of the increased availability of the technology and the system performance advantages it provides.

Some of the specific highlights of 1986 are described below. References are included to the sections of this report where more information may be found.

o   The first demonstration of VHSIC technology in an operational environment took place in July 1986. Portions of the AN/ALQ-131 electronic warfare pod were redesigned by TRW to take advantage of its Phase 1 VHSIC chips. The new design can be retrofitted into the existing system to provide increased reliability, easier maintenance, simplified system operation, and reduced weight and space for the electronics. In July, prototype production hardware using VHSIC was flight tested at Eglin AFB. [Section III.3]

o   In September, the Navy demonstrated the field installation and flight operation of a VHSIC Signal Conditioner (VSC) for the AN/UYS-1 ASW sonobuoy equipment aboard a P-3 aircraft. The VSC doubled the capacity of the AN/UYS-1 with no other changes in the system configuration. [Section III.2]

o   In December, the Army conducted a laboratory demonstration of VHSIC components in the Enhanced Position Location and Reporting System (EPLRS). The insertion of VHSIC into the signal and message processing module of EPLRS results in a multimode waveform capability which can be used either to triple the data throughput or to increase the jamming margin. [Section III.1]

o   The VHSIC Hardware Description Language (VHDL) has emerged as a major vehicle for the interchange of VHSIC/VLSI design information, specifica-

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[1] The term "micron" is commonly used in place of the standard term "micrometer" which is equal to 10^{-6} meters. See the glossary in Appendix VI for a list of other acronyms and technical terms.

tions, and functional descriptions as well as for CAD tool operation. Steps are being taken to adopt VHDL as a national design standard through cooperation with the IEEE. [Section V.1]

o The yield enhancement program, aimed at improving the manufacturability of VHSIC chips, has resulted in multiprobe yields as high as 83% for a 72K memory and 41% for an arithmetic logic unit. By the end of 1986 twenty nine fully functional VHSIC chip types had been fabricated and the total production of VHSIC chips exceeded 100,000. [Section II.2]

o Five production lines have been certified for the manufacture of VHSIC products in accordance with DoD standards. In addition, contracts have been awarded to qualify seven of the VHSIC chips to military specifications and place them on the DoD Qualified Products List during 1987. [Section II.3]

o The 1986 Annual VHSIC Conference was held at the Johns Hopkins University Applied Physics Laboratory on December 9-11. At the Conference, twenty organizations displayed information on products related to VHSIC. Of these exhibitors, sixteen showed facilities capable of producing VHSIC chips. [Appendix III]

o A demonstration of the potential for an automated "VHSIC factory of the future" was made by coupling the output of a silicon compiler program to the VHSIC pilot production line at National Semiconductor Corporation. The first silicon wafers using this procedure have been successfully produced with a 54% yield of operating test chips. [Section V.1]

o The first AEBLE-150 electron beam lithography machine, developed in the Phase 1 program by Hughes Research Laboratory and Perkin Elmer Corporation, was delivered in October to Motorola for use in the production of Phase 2 submicron chips. The machine has been set up at Motorola and is undergoing exhaustive testing during which an up-time of 70-80% has been experienced. [Section V.2]

o Three Phase 2 chips designed by IBM for the submicron program have been successfully fabricated. Two of them have already passed functional tests showing that they operate as designed. These chips are designed initially with 1.0 micron dimensions and will be reduced to 0.5 micron after further functional testing. [Section IV.2]

o The Phase 2 contractors - Honeywell, IBM, and TRW - have established an interoperability specification which will ensure that functional modules built with VHSIC chips are able to exchange data, control, and test/maintenance signals. [Section IV.2]

BACKGROUND

In March 1980, the Department of Defense began the Very High Speed Integrated Circuits program for developing advanced silicon integrated circuits.

Prior to that time, the DoD had spent several years carefully assessing its needs and deficiencies in this area of technology. The major deficiency perceived was that the DoD procurement of state of the art microelectronic products was running ten or more years behind their appearance in the commercial market. Worse still, the delay was increasing with time. However, the need for ready access to this technology had become increasingly vital to the U.S. defense posture as the weapon systems being deployed became more and more dependent on electronic subsystems for their effectiveness, for their speed of response, and for their adaptability in rapidly changing battle environments. The goal of the VHSIC program was, and still is, to correct that deficiency by giving system developers and acquisition managers a military qualified microelectronic technology that was on par with or better than the technology available commercially.

PHASE 1

Following one year concept definition studies by each of nine contractors, the first phase of the technology development effort began on May 1, 1981. This Phase 1 effort concentrated on developing a microelectronic chip technology characterized by feature sizes as small as 1.25 microns and a minimum operating frequency of 25 MHz. The prime contractors selected for Phase 1 were Honeywell, Hughes Aircraft, IBM, Texas Instruments, TRW, and Westinghouse. Each of the contractors defined one or more VHSIC chips which they would design, fabricate, and then demonstrate in a simulated operating environment. A total of twenty eight VHSIC chips were defined at first. Two more were added later. In 1983 the first VHSIC chip was successfully fabricated and by the end of 1986 twenty nine of them had been produced on the VHSIC pilot lines and operated as designed.

The first VHSIC chips were produced at yields generally averaging less than 1%. Beginning in 1984, additional efforts were begun at each of the contractors to increase the yield of the VHSIC chips to the point where their manufacturability at a reasonable cost was assured. This program resulted not only in greatly increased yield for all of the VHSIC chips but also in a considerable stock of produced chips. Figure ES.1 at the end of this summary shows the current status of VHSIC chip yield. Other semiconductor producers have been stimulated by these successes to design and fabricate VHSIC-class chips so that the VHSIC technology is becoming more widely available.

TECHNOLOGY INSERTION

The VHSIC program has supported the insertion of VHSIC chips into actual military systems, including existing, fielded systems and those still under development. In cooperation with the system program offices, VHSIC has funded both feasibility studies and hardware demonstrations in operating systems. At least twenty seven major system insertioon efforts are beiong undertaken in which the use of VHSIC technology provides the potential for improved system performance. In some cases such as the Army's FIREFINDER radars and the joint Navy/Air Force HF/EHF communications terminal, the projected saving in system life cycle costs approaches the total cost of the VHSIC program.

During 1986, VHSIC chips were flight tested in the AN/ALQ-131 airborne electronic warfare pod, field demonstrated in the AN/UYS-1 airborne anti-submarine warfare suite, and laboratory demonstrated in prototype hardware of a man-carried position location and reporting system (EPLRS).

PHASE 2

With the successful development of the 1.25 micron technology and its transition into manufacturable products largely accomplished, the VHSIC Program Office initiated the Phase 2 submicron program aimed at developing a second generation of silicon chips that are characterized by 0.5 micron feature sizes and a clock frequency of 100 MHz. The contractors selected to undertake the submicron development tasks are Honeywell, IBM, and TRW. Contracts were awarded in November 1984 and the program is now halfway through the scheduled four year effort. Honeywell is developing a bipolar fabrication process and designing two large gate array chips for use in an advanced electro-optical image processor module. IBM is using a CMOS process to build three chips, first with 1.0 micron minimum dimensions and then with 0.5 micron dimensions. The demonstration module for these chips is a beamformer for a large sonar array. TRW is working on a "superchip" design concept with 0.5 micron CMOS technology. Using highly redundant circuit blocks in order to increase the projected manufacturing yield, TRW is designing chips as large as 1.5 square inches and containing over 20,000,000 transistors. In addition to the signal processing chips, each of the contractors is committed to design and build a bus interface unit which has a standard set of signal protocols and other interface parameters so that the Phase 2 demonstration modules can communicate with each other.

PHASE 3

In addition to the primary chip development efforts in Phase 1 and Phase 2, the VHSIC Program Office has found it necessary to include in the program a number of independently funded contracts for the development of supporting technologies. These efforts included advanced high resolution lithography, automated design aids, improved materials, self testing and fault tolerant design, packaging, and testing. These contracts are collectively called Phase 3 of the VHSIC program.

An advanced electron beam lithography machine was developed by a Hughes Aircraft/Perkin Elmer team during the Phase 1 time period. This machine was designed to produce 0.5 micron feature chips at a rate that would make their production economically feasible. The first production model of this machine was delivered to Motorola in October 1986 for use on the Phase 2 submicron program.

The electron beam machine development was undertaken to provide a high resolution system that could go well beyond the fundamental limitation of optical wavelengths. VHSIC has also supported the development of an advanced optical lithography machine and both IBM and Motorola are independently working with new commercial optical equipment and finding that such equipment can produce large VHSIC size chips with resolution in the 0.7 to 0.8 micron range. It appears that by the end of the Phase 2 program it may even be possible to produce 0.5

micron VHSIC chips optically.

The level of complexity of VHSIC chips ranges from about 20,000 transistors for the simplest Phase 1 chips, to over 20,000,000 for the TRW Phase 2 super-chips. The use of computer aided design (CAD) tools is absolutely required to design, analyze, check, interconnect, lay out, fabricate, and test such a complex system. VHSIC has undertaken to develop some of the necessary tools to do this within the framewoi k of IDAS - the Integrated Design Automation System. The cornerstone of IDAS is the VHSIC Hardware Description Language (VHDL). VHDL provides a common language for transmitting design information between the various CAD tools and for uniform documentation of the designs of different organizations. VHDL is in the process of being adopted as a national standard for this purpose. During 1986, a number of IDAS tasks were undertaken to validate the VHDL at several beta sites and to extend existing design tools from the circuit and logic level into the system architecture level. The VHDL language is currently implemented on the VAX series of minicomputers, but a joint U.S./Canadian program has been started to adapt the VHDL to IBM mainframe computers.

MANAGEMENT

In 1984, the VHSIC Program Office began a program for making people in the system community more aware of the new electronic technology being developed in VHSIC and to train engineers in its use. Since then thirty VHSIC Application Workshops have been held throughout the nation, extended training seminars have been organized, and a variety of training documents have been written. Both the Air Force Institute of Technology and the Johns Hopkins Applied Physics Labora-tory are offering courses on VHSIC design methodology.

To further encourage the wide spread use of VHSIC in the design of military systems and yet control the undesired diffusion of the technology beyond the areas of U.S. interest, the DoD has formalized several policy positions. Each of the Services has prepared transition plans for the insertion of VHSIC technology into current and future systems. DoD Instructions 5210.75 and 5230.26 establish the policy and provide the guidelines for the handling and control of VHSIC information and products.

Section I of this report reviews in more detail the background, origins, and structure of the VHSIC program. Sections II through VI cover, in sequence, each of the major subdivisions of the program:

o Phase 1 - development of 1.25 micron technology
o Technology Insertion - in selected military applications
o Phase 2 - development of 0.5 micron technology
o Phase 3 - supporting technologies
o Management - training, technology transfer, security

In each of these sections, the program activity through 1985 is covered briefly. Then the progress, achievements, and status for 1986 are described. The appen-

dices provide a list of major reference documents pertaining to VHSIC, a list of current and completed VHSIC contracts along with contacts for more complete information, a list of the exhibitors at the 1986 Annual VHSIC Conference, copies of the Statements of Work for Phase 1 and Phase 2, and a compilation of the acronyms and technical terms used in the report.

FIGURE ES.1

<u>VHSIC PHASE 1 CHIP YIELD STATUS (12/86)</u>

COMPANY	CHIP	Multiprobe Yield %	GOAL %
Honeywell	Sequencer	25	13.6
	Pipeline Programmable Processor	13	
	Arithmetic Unit	16	
Hughes	Correlator	7	10
	Encoder/decoder	>15	
	Signal Tracking Subsystem	2	
	20K Gate Array	–	
IBM	Complex Multiply/Accumulate	11	4
	Signal Processingg Element	34	12
T.I.	Static RAM (72K)	83	12
	Vector Arithmetic Logic Unit	7	
	Vector Address Generator	27	
	Array Controller/Sequencer	43	11
	Data Processing Unit	36	
	Multipath Switch	41	
	General Buffer Unit	19	
TRW	Window Addressable Memory	11	5.7
	Content Addressable Memory	10	6.6
	Matrix Switch	62	
	Register Arithmetic Logic Unit	20	
	Multiply/Accumulate	9	
	Address Generator	37	
	Four Port Memory	15	8.8
	Microcontroller	15	
Westinghouse	Static RAM (64K)	26	10
	Static RAM (16K)	78	
	10K Gate Array	36	
	General Purpose Controller	–	
	Extended Arithmetic Unit	–	
	Pipeline Arithmetic Unit	–	

SECTION I

THE VHSIC BACKGROUND

I.1 INTRODUCTION

The acronym "VHSIC" stands for "VERY HIGH SPEED INTEGRATED CIRCUITS". It is the name of the Department of Defense program to develop two new generations of silicon integrated circuits. These ICs will supply the higher performance electronics needed by the DoD in its weapon systems.

This report summarizes the background of the VHSIC program and the main contract efforts being undertaken to accomplish the program objectives. Some of the prior accomplishments which have been made through 1985 are reported along with a more detailed description of the major activities carried out during 1986.

The technical efforts of the VHSIC program are focused on using the best available materials, techniques, and equipment to make advanced silicon ICs. These silicon ICs are the only feasible technology currently available for solving the demanding problems of signal processing, data transfer, and weapon control that arise in the operation of modern military weapon systems.

However, the goals of the VHSIC program go beyond the technical tasks involved in the design and fabrication of these highly complex ICs. The ultimate objective is to bring them to a production status for early and affordable use in weapon systems. The early deployment of such superior technology will preserve and even extend the military superiority of the U.S. in world conflicts. In order to achieve this goal the products of the VHSIC program must meet at least the following criteria:

- o be available for procurement at least as soon as comparable commercial products,
- o be significantly lower in projected life cycle cost than current technologies,
- o have higher reliability for the same function,
- o be producible to military standards and specifications, and
- o have a short design/fabrication cycle time.

In order to accomplish these goals the VHSIC program has marshaled the efforts of a significant portion of the U.S. electronics industry. The work has included research in new materials and processing techniques, the development of new equipment for the fabrication of extremely complex circuits, exploration of new ways to bring computer automation into the design of these circuits, and a major effort at bridging the gap between the development of a new level of technology and its practical use in military equipment under operational conditions.

Appendix I lists the more important technical reports issued thus far and other references relevant to the program. Appendix II lists all of the major contractors for the various phases of the VHSIC program along with key personnel both in industry and in the Government.

Program Rationale

The defense posture of the United States is increasingly based upon the concept of a military force that is technologically superior to any potential adversary. We use technology wherever possible to ensure our ability to defend against numerically greater forces. The technology of the integrated circuit has become the foundation of the complex electronic systems that are employed as force multipliers in our Nation's defense. It is essential, then, to keep our technology well ahead of that available to potential adversaries.

In the past we were able to maintain a comfortable lead in the military applications of integrated circuits. However, by the late 1970's it became apparent that our 'comfortable' lead had seriously eroded. As a result our ability to maintain a superior military force, assisted by the earlier access to advanced electronic technology, was in question.

One of the major reasons for this erosion of capability was that it was taking longer and longer for the DoD to move high performance ICs from the development laboratory into military systems. Commercial use of a given level of IC technology, by contrast, often preceded military applications by as much as 8 to 10 years. Military weapon systems were becoming technologically obsolete before completing their expected logistic life span. The security and integrity of our future military capabilities were jeopardized. Four major factors contributed to this situation.

o By 1978, the military share of the IC industry market had dwindled to approximately 7%. Manufacturers thus were giving priority to commercial needs rather than to military requirements.

o The cost of designing and producing military ICs had increased disproportionately with time. The small quantities involved in military procurement resulted in much higher unit costs compared to commercial orders.

o The rapid evolution of new IC designs and production technologies caused early obsolescence of specific parts and the facilities that produced them. This caused severe logistic repair and maintenance problems for fielded systems.

o Military system program managers were cautious about applying new IC technology in a system development which was subject to limited program funds and fixed time schedules.

The impact of these factors can be illustrated graphically. The life cycle of a semiconductor technology has four distinct phases, each with its own characteristic level of production.

During the development and design phase the production is very low – primarily for testing and evaluation of the parts. As the technology moves into prototype system applications the production increases to supply the parts needed for building the systems which are committed to this technology. During the third phase full production is achieved as the technology is accepted for use in systems and demand for it remains high. Then, as newer products are success-

fully developed and put into production they supersede the older generation. In this fourth phase the semiconductor product is gradually withdrawn from production and becomes obsolete. The length of time from the beginning of the first phase to the end of the last phase is currently about four years for a commercial product. This period represents the average market lifetime of a specific product.

If this life cycle evolution is compared to the acquisition cycle for military systems, as shown in Figure I.1, the increasing disparity with time between the technology cycle and the production cycle can be seen. In the late 1960s, during the Small Scale Integration era, the Advanced Development (6.4) and production stages for the system took place while IC production was still high. In the early 1970s the system acquisition time had stretched out and the available Medium Scale Integration products were entering a declining production phase by the time the system was ready for deployment. By the late 1970s when Large Scale Integrated circuits were being procured for fielded systems, they were already being superseded on the production line by more advanced technologies when system production began.

Figure I.2 illustrates what the VHSIC program hopes to achieve. The life cycles of three generations of VHSIC technology are expected to have the same pattern of growth-production-decline as previous semiconductor developments. The three generations include the VHSIC Phase 1 technology which is becoming available now; the Phase 2 submicron effort which is expected to be finished by 1990; and the follow-on programs beyond VHSIC which will extend into the 1990s. Each of these generations can be integrated into all DoD weapon systems regardless of their stage in the acquisition cycle. Through aggressive system development and support, the protracted and interrupted system acquisition cycle can be reduced to its original time span. The system acquisition cycles depicted in Figure I.2 do not represent specific systems, but rather systems at each milestone spanning the acquisition cycle from R&D (6.2) on new systems to operation and support of older systems already in the field.

In summary, the VHSIC program has set as its goal a sharp reduction in the delay experienced by the DoD in getting advanced, state-of-the-art ICs into military usage. As Figure I.3 shows, this delay has grown steadily for more than a decade so that today it is typically the commercial market rather than the DoD that introduces the new generations of semiconductor technology. Ultimately new IC usage in the DoD should take place in pace with (or perhaps even before) its appearance in the commercial market place.

In order to accomplish its tasks and reach its goal the DoD must do more than solve the "catch-up" problem for one or two generations of new ICs. VHSIC must put into place within the U.S. semiconductor industry a capability to do this on a continuing basis. It must be able to take into account the short life expectancy of any given generation of IC products. It must also plan for and lead the development of IC products designed specifically for military usage - i.e. where little or no commercial usage is expected. The VHSIC program has been structured to do this within two IC generations. The first generation is now being produced and is demonstrating that the DoD can, in fact, accomplish these tasks.

References I.10 through I.22 provide further background information on the origins, structure, and rationale of the VHSIC program.

DEPLOYMENT OF TECHNOLOGY INTO SYSTEMS

— THE OLD WAY (CIRCA 1977)

12

—THE VHSIC WAY (CIRCA 1985)

BEYOND VHSIC

PHASE 2 (0.5μ)

PHASE 1 (1.25μ)

NEW SYSTEMS

| 6.2 | 6.3 | 6.4 | PROD | O&S |

| | 6.2 | 6.3 | 6.4 | PROD | O&S |

| | | 6.2 | 6.3 | 6.4 | PROD | O&S |

| | | | 6.2 | 6.3 | 6.4 | PROD | O&S |

OLDER SYSTEMS

| | | | | 6.3 | 6.4 | PROD | O&S |

TIME

13
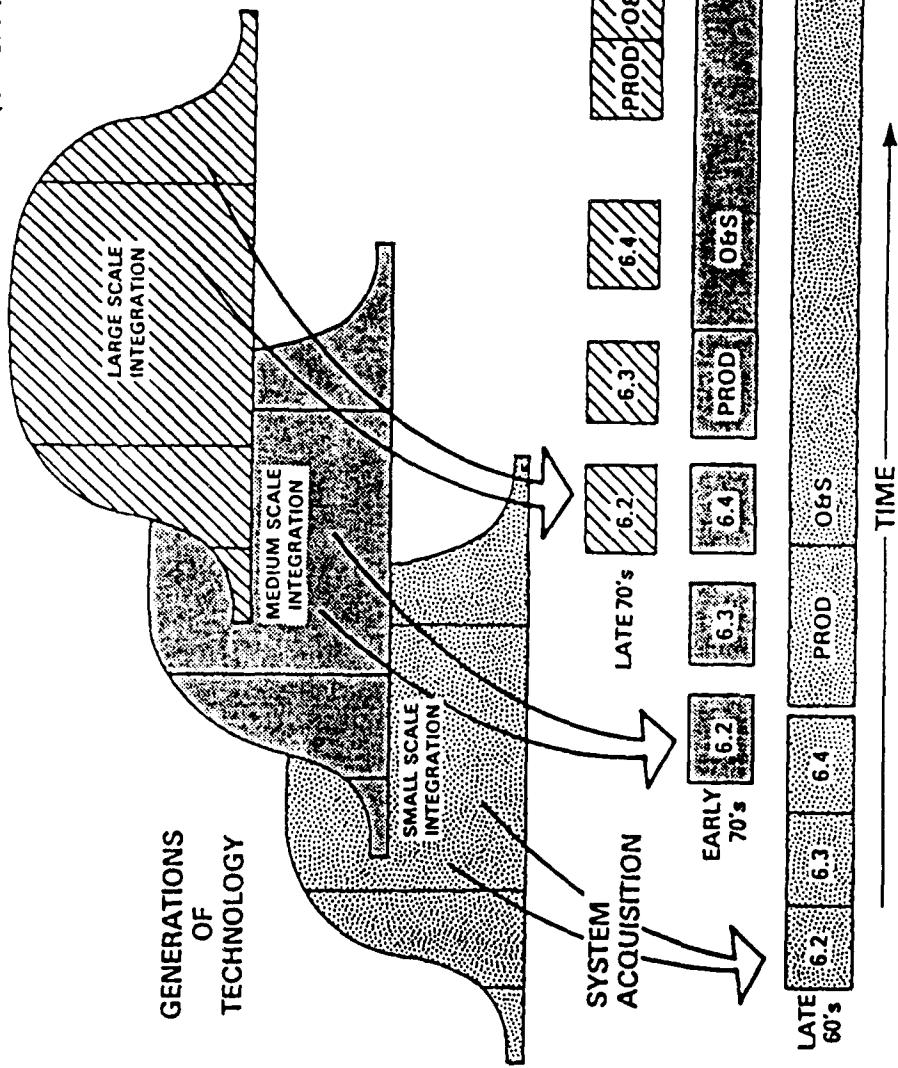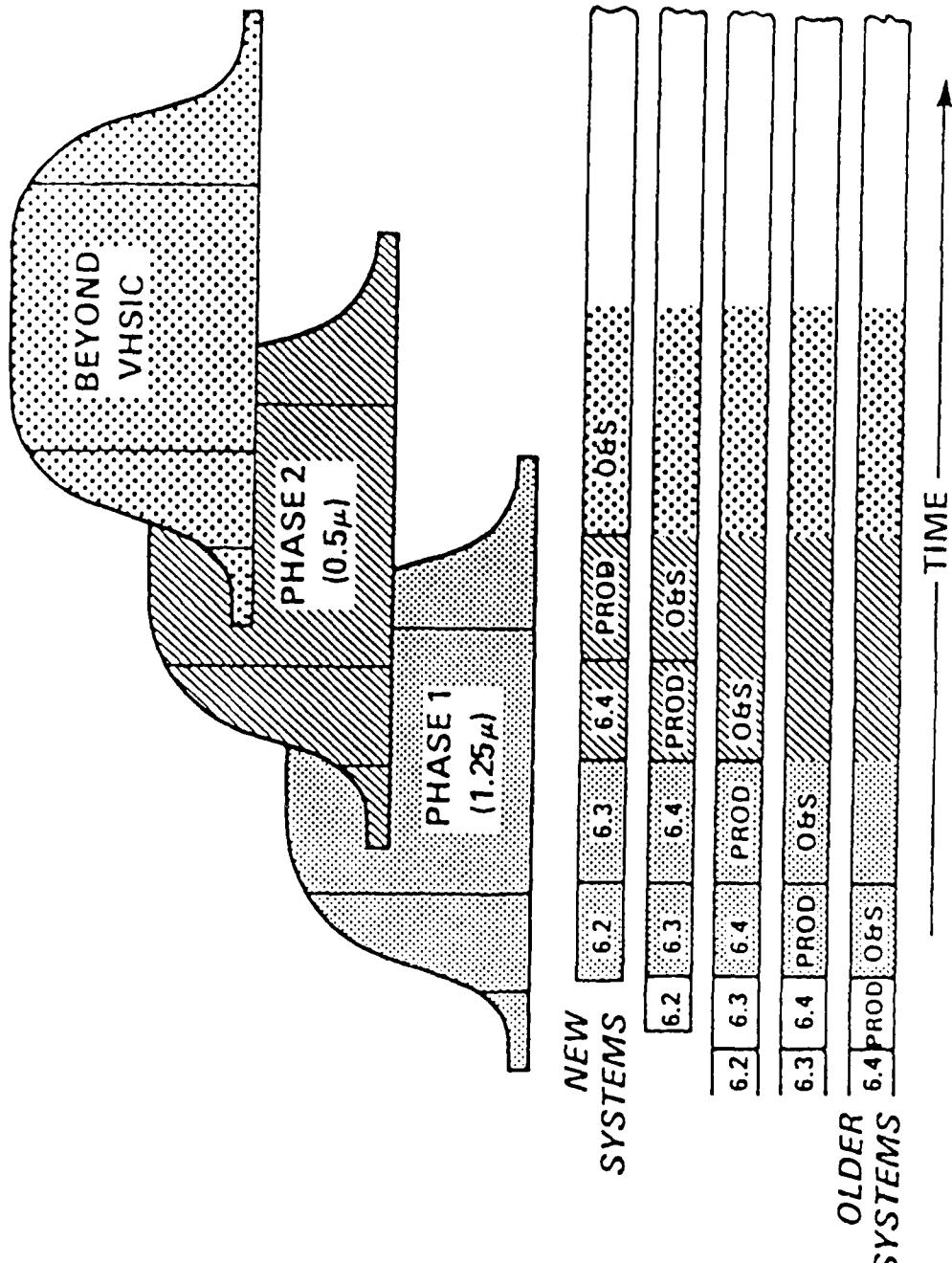
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MILITARY SYSTEMS LAG COMMERCIAL SYSTEMS
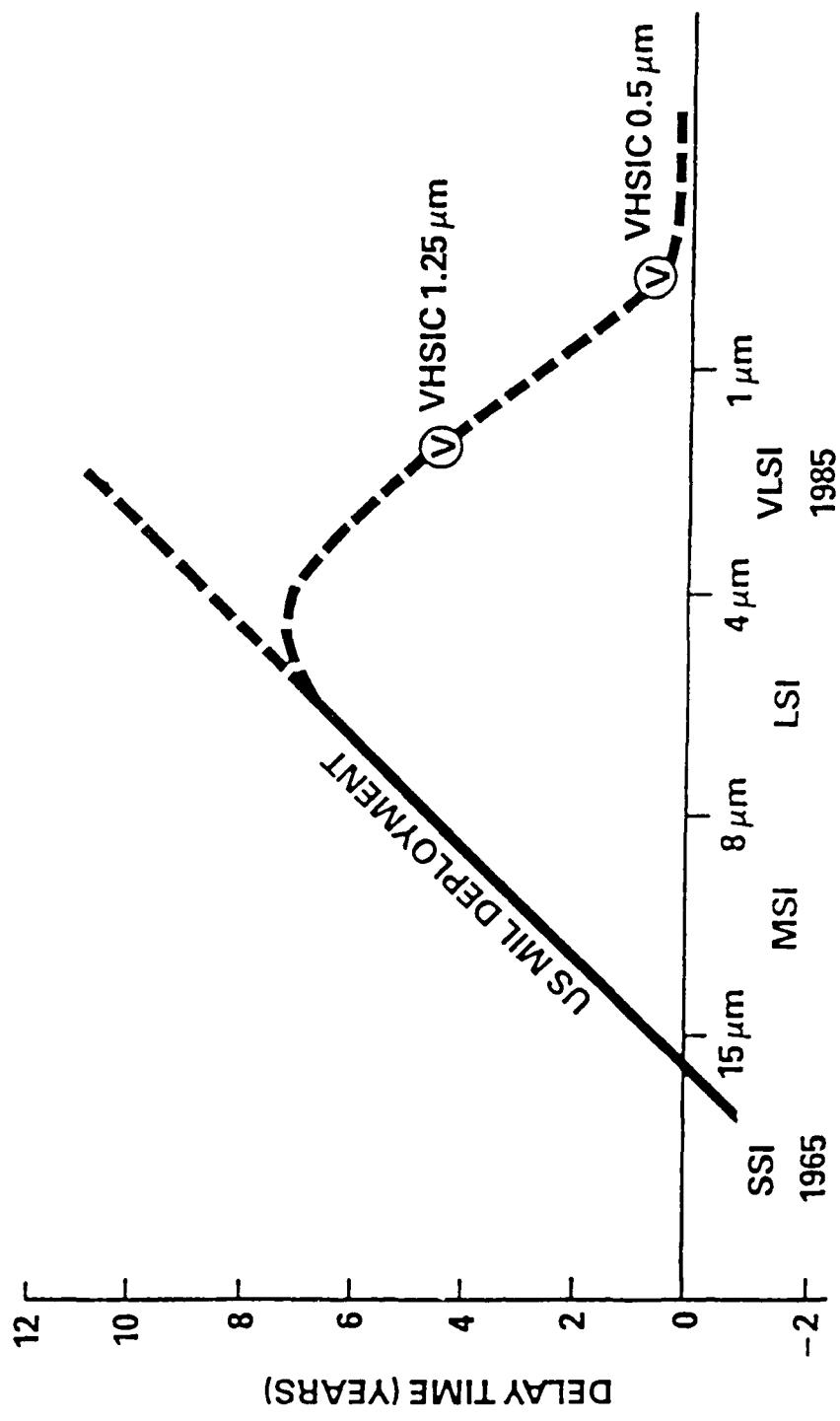
VHSIC Program Structure

The DoD recognized at the start that the VHSIC program had to address both technical and management problems. The primary technical task would be to develop military specific ICs. At the same time, a level of security and control was necessary in order to prevent compromise of the program and its goals. In 1978, the DoD adopted a management plan which would:

o establish the VHSIC Program Office within the Office of the Secretary of Defense supported by similar offices in the Army, Navy and Air Force,

o develop an industrial contracting program for two new genera ons of advanced integrated circuits specifically designed to meet military system needs and provide the capability to support long term use of the circuits,

o initiate an aggressive program to insert this technology into systems in such a way that it would minimize the financial and schedule risks to the weapon system developer,

o provide leadership and guidance for the semiconductor industry to develop a VHSIC production capability that would continue to meet specific military needs while complementing the commercial goals of semiconductor manufacturers,

o operate the program under the International Traffic in Arms Regulations (ITAR) to ensure adequate security control.

The VHSIC Program Office was established in the Office of the Under Secretary of Defense for Research and Engineering whose functions have since become part of the Office of the Under Secretary of Defense for Acquisition. With the assistance of Program Directors from each of the three Services, the VHSIC Program Director manages overall technical, financial and policy matters. Day-to-day contract management and technical expertise are provided by the three Services, under the leadership of the Service Program Directors. Together they conduct frequent program reviews and monitor the overall technical progress of contractors in each of the various phases of the program. Several other Defense agencies work in cooperation with the VHSIC Program office to assist in solving specific problems.

The structure of the VHSIC program evolved from a number of considerations. The ultimate technical goal was to be able to design, make, and use silicon ICs that were more advanced than any commercially available. After a number of

discussions between Government and industry representatives, the goals of one-half micron feature size and 100 megahertz speed were chosen as reasonable quantifiers of the desired product. IC chips combining these two characteristics would imply the ability to do electronic signal processing much more effectively than current technology. However, it was also felt that these goals (plus other device parameters described below) could only be reached after prolonged development efforts.

An intermediate, "mid-term" goal of 1.25 micron feature sizes and 25 megahertz clock speed was chosen. This goal would be much less difficult to meet but would still be a significant advance in technical capability. It would also lessen the risk of the program and, if necessary, provide a decision point midway through the program on whether to proceed or not. During the development of plans for the VHSIC program it was evident that many of the detailed technologies involved in IC design, fabrication, and use were sufficiently new that supporting R&D in these areas was needed in order to reduce the risk of the main line of development.

It was also obvious from the start that the wide spectrum of capability in the U.S. semiconductor industry and the equally wide technical approaches possible toward achieving the program goals would make it impossible for the Government by itself to define the detailed tasks necessary to initiate a full scale development program. The DoD would need close interaction with industry in putting the program into action. It decided to do this by means of a concept definition phase in which many contractors would be funded to study the problems posed by the VHSIC goals and to describe in detail their approach to solving them.

The program structure that evolved from all of these considerations is shown in Figure I.4 and includes four complementary phases.

PHASE 0 - March 1980 to March 1981: a one year effort to conduct intensive preliminary studies and then define a detailed development program to accomplish the technical objectives set out by the VHSIC program office. Emphasis was put on 1.25 micron minimum feature size and 25 megahertz clock speed. Nine companies participated in Phase 0.

PHASE 1 - May 1981 to May 1984: a three year primary effort on development and pilot production of silicon chips with 1.25 micron minimum feature sizes and their demonstration in subsystem brassboards. Phase 1 contracts were awarded to six major companies, or teams, with expertise in weapon systems development and semiconductor manufacturing.

This phase was later expanded with the addition of an aggressive technology insertion program and a yield enhancement program. The insertion program initially included the requirement for the development of an integrated design automation system (IDAS). However, IDAS proved to be particularly important to the long term goals and it has become a separate program effort. These added activities were necessary to ensure sustained and cost effective application of 1.25 micron technology.

VHSIC PROGRAM ROAD MAP

FY 80	FY 81	FY 82	FY 83	FY 84	FY 85	FY 86	FY 87	FY 88	FY 89

PHASE 1 TECHNOLOGY INSERTION

1.25μ PROGRAM DEFINITION

PHASE 1

TECHNOLOGY DEVELOPMENT

PILOT LINE ESTABLISHMENT

BRASSBOARD FABRICATION

PRE-INSERTION STUDIES

SPECIFIC SYSTEM DESIGN/NEW CHIPS

PHASE ONE YIELD ENHANCEMENT

MANUFACTURING TECHNOLOGY

VHDL DEFINITION

DESIGN AUTOMATION

SUBMICRON TECHNOLOGY

0.5μ PROGRAM DEFINITION

TECHNOLOGY DEVELOPMENT

PILOT LINE ESTABLISHMENT

BRASSBOARD FABRICATION

BRASSBOARD FABRICATION

EARLY PHASE 3

LATE PHASE 3

LITHOGRAPHY/MATERIALS/QUALIFICATION/HARDENING

17

PHASE 2 - October 1984 to November 1988: a four year primary effort on the development and pilot line production of silicon chips with 0.5 micron minimum feature size and 100 megahertz clock speed and for their demonstration in subsystem modules by the end of 1988. Three prime contracts for this phase were awarded in October 1984. This phase was preceded by another concept definition study (Phase 0') similar to Phase 0, in which detailed approaches to the 0.5 micron goal were developed and proposed by nine contractor teams.

PHASE 3 - FY 1980 to FY 1989: a variety of efforts dedicated to solving the technical problems that have been identified during pursuit of the main program objectives. Specific efforts have been undertaken to deal with technology applications, materials requirements, lithography and fabrication tools, design software development, packaging, chip qualification, and radiation hardness.

Under the management function of the VHSIC Program Office, a vigorous training and awareness program has been conducted. In addition, there has been a growing activity in the transfer of VHSIC information and products to weapon system developers in the industrial and Government defense community.

The structure and goals of the VHSIC program express DoD's confidence in the ability of industry to provide superior IC technology and production capacity for use by the military in a timely and cost effective manner. By establishing the VHSIC Program Office within the Office of the Secretary of Defense, with full participation of the Army, Navy, and Air Force, DoD ensured the support and resources necessary to accomplish the program goals.

The first insertion of VHSIC into an operational weapon system (AN/ALQ-131 electronic warfare system) occurred in December 1985. It demonstrated that DoD can put state of the art electronic technology into military systems as quickly as they are put into commercial systems.

I.2   PHASE 0 - CONCEPT DEFINITION STUDY

The problems that had gradually arisen in military microelectronics were recognizable and the goals of a program to solve them were readily stated. However, the most rational and orderly direction to take for achieving those goals was neither apparent nor unique. Different opinions were expressed on what should be done, who should do it, how fast to proceed, what level of technology to pursue (basic research, development, or manufacturing technology), what the technical objectives should be, and other programmatic questions. Since the system capabilities needed by the DoD had to be developed by and reside in industry, the DoD turned to industry for help in defining the details of the VHSIC program. The mechanism for doing this was a Phase 0 Concept Definition Study effort. The use of contractual concept definition efforts is well established and very effective for defining large, a complex program before making a final commitment to it.

The procedure for Phase 0 was for each of a number of contractors to describe in detail an approach to meet the VHSIC goals. Emphasis was placed on signal processing applications, but data processing applications were not excluded. Specifically, Phase 0 was to provide sufficient system analysis, design layouts, computer aided device modeling, and experimental work to define a detailed approach to the VHSIC problems.

Phase 0 was intended to be primarily a study effort in which innovative approaches to any of the multitude of technical problems would be encouraged. It was not intended that extensive experimental work be done during this phase or that detailed circuit designs and layouts would be produced. Existing fabrication processes could be characterized in more detail to define the parameters and requirements for further work. However, the development of new processes was not required.

At the end of Phase 0, each of the competing contractors would present a plan for proceeding on to three or more years of intensive development effort. The Government would then select those plans which it judged most likely to meet the ultimate objectives of the VHSIC program successfully.

As guidance during the Phase 0 studies, the VHSIC Program Office required the IC technology to meet the following specifications:

o functional throughput rate of 5×10^{11} gate-Hz/cm^2,

o on-chip clock rate of at least 25 MHz,

o minimum feature size of 1.25 microns,

o operation over the temperature range of -55°C to +85° C [However, operation over the full military temperature range of -55°C to +125°C was considered the ultimate goal of VHSIC devices.],

o operation without radiation induced failures in a radiation environment of at least 10^4 rads(Si) with 5×10^4 rads(Si) as a goal,

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o operation without radiation induced permanent failures after a transient radiation dose during operation of at least 10^8 rads(Si)/s with 10^9 rads(Si)/s as a goal (for a 100 nanosecond pulse),

o operation without transient upset through a radiation pulse of 10^7 rads(Si)/s (for a 100 nanosecond pulse),

o operation without permanent damage after a neutron radiation dose during operation of at least 10^{11} neutrons/cm^2, (1 MeV equivalent), and

o failure rates not exceeding .006% per 1000 hours at 60% confidence level (end goal).

Each of the Phase 0 contractors was required to provide information and proposals in the following areas:

o electronic subsystem candidates for possible implementation as VHSIC brassboards,

o identification of broadly applicable VHSIC chips required by the subsystem candidates,

o architecture of the required VHSIC chips and approaches to their design,

o chip fabrication technology and processing techniques needed to make VHSIC chips with 1.25 micron and submicron minimum features,

o definition of a packaging approach for both 1.25 micron and submicron chips,

o computer aided design (CAD) requirements,

o lithographic requirements for the fabrication of 1.25 micron and submicron devices,

o key processing equipment that needed to be developed,

o existing and/or any proposed facilities necessary to meet VHSIC design and fabrication requirements,

o support systems such as a higher order language in DoD systems which would simplify the use of VHSIC,

o approaches to providing increased reliability and testability of VHSIC devices,

o procedure for making VHSIC products available for sale to all other DoD contractors and government laboratories,

o   procedure for making major equipment developed available to other DoD contractors and government laboratories, and

o   corporate strategy for rapidly introducing VHSIC into DoD systems.

Fourteen industry teams submitted proposals for participation in Phase 0. The study programs were completed in December 1980. Final technical reports for each of the contracts are listed in Appendix I. Based on the work during the Phase 0 contracts, each company submitted a proposal to the Government for Phase 1 emphasizing the development of 1.25 micron technology and a brassboard which would demonstrate the advantages of its application in systems.

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FIGURE II.1 (Continued)

VHSIC PHASE 1 CONTRACTS

ORGANIZATION	CHIP SET	FEATURES
Texas Instruments $22.7M	Vector Arithmetic Logic Unit Vector Address Generator Data Processing Unit Multipath Switch Array Controller/Sequencer Device Interface Unit General Buffer Unit Static RAM	Multimode fire and forget missile brassboard ROM programmable chip architecture Bipolar Schottky transistor logic, NMOS memory Multimaster synchronous parallel bus Leadless chip carrier package Design utility CAD system
TRW (prime) Motorola Sperry-Univac $34.6M	Content Addressable Memory Window Addressable Memory Address Generator Register Arithmetic Logic Unit Microcontroller Multiply/Accumulator Matrix Switch Four Port Static RAM	Electronic warfare brassboard Hardwired custom chip set 3D bipolar technology for logic CMOS technology for memory Multidrop interconnect bus Chip carrier with 132 leads, 25 mil centers Hierarchical CAD system
Westinghouse (prime) National Semicon Control Data Harris Carnegie-Mellon	Controller Pipeline Arithmetic Logic Unit Extended Arithmetic Logic Unit Extended Arithmetic Unit Multiplier 10K Gate Array Static RAM	Airborne multimode radar processor brassboard Hierarchical multiprocessor architecture Programmable high performance chip set CMOS technology for all chips High speed ring bus network Wire/tape bonding; 44,160,220 lead packages; multi-layer ceramic flatpack with 20 mil centers

FIGURE II.1

VHSIC PHASE 1 CONTRACTS

ORGANIZATION	CHIP SET	FEATURES
Honeywell $19.9M	Parallel Pipeline Processor (PPP) Sequencer Controller	Electro-optical signal processor brassboard Parallel pipeline architecture Bipolar integrated Schottky and current mode logic Multimaster high speed local bus and medium speed global bus with serial arbitration Ceramic beam lead tape chip carrier package, up to 240 leads, pin and pad array options
Hughes $37M	Digital Correlator Algebraic Encoder/decoder Signal Tracking Subsystem	Battlefield information distribution brassboard Electronically reconfigurable chips CMOS/SOS technology Pipeline interconnects Leaded flatpack, 148 pin, 25 mil centers Hierarchical CAD in VAX
Hughes (prime) Perkin Elmer $8.1M	Electron Beam Lithography Machine	High throughput 0.5 micron lithography, 0.1 micron resolution
IBM $19.9M	Complex Multiplier/Accumulator	Acoustic signal processor Master image with primitive and custom macrocells NMOS technology Pipeline on chip Controlled collapsible chip connection with polyimide decal Multilayer ceramic package CAD tool set in place

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o Define the CAD tools needed to support the full spectrum of the design process from architectural specification to physical chip interconnection and layout.

o Develop a simulation methodology to validate circuit, chip, and subsystem designs and to project performance accurately before fabrication.

(3) Chip and subsystem design

o Carry out a detailed system analysis to define the VHSIC subsystem design requirements.

o Develop specifications for the VHSIC modules, chips, and functional macrocells.

o Design and layout the VHSIC chips and modules needed for the brassboard, including provision for testability and fault tolerance.

o Demonstrate the completed brassboard in simulated operational conditions.

(4) Technology transfer

o Provide an effective plan for making chips, design services, equipment, and software available to other DoD contractors.

o Establish a plan for developing a second source of supply for chips.

o Prepare a plan for insertion of the VHSIC technology into DoD systems.

The primary performance requirements for the chips to be produced in Phase 1 are listed below. More desirable levels were listed as goals if in the course of the program the technology became achievable. The detailed requirements are listed in Appendix IV.

Functional throughput rate	5×10^{11} gate-Hz/cm^2
Minimum feature size	1.25 microns
On chip clock speed	25 MHz
Temperature	-55°C to +85°C (+125°C goal)
Radiation (total dose)	10^4 rads(Si) (5×10^4 goal)

The technical aspects of the Phase 1 contracts at the start of the program in May 1981 are summarized in Figure II.1. More detailed characteristics of the chips proposed by each of the contractors is shown in Figure II.2. The major program accomplishments over the past five years are briefly described for each of the six contracts. Detailed information can be found in the technical reports submitted by the contractors and available through the Defense Technical Information Center. These documents are listed in Appendix I and referenced, where appropriate, throughout this report. A full list of the contractors, contract numbers, and program managers in included in Appendix II.

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SECTION II

PHASE 1

II.1 PHASE 1 - 1.25 MICRON TECHNOLOGY DEVELOPMENT

In December 1980, the nine Phase 0 contractors submitted proposals to the DoD to perform the tasks designated for Phase 1. The contractors were General Electric, Honeywell, Hughes, IBM, Raytheon, Rockwell, TRW, Texas Instruments, and Westinghouse. The proposals were evaluated and in May 1981 contracts were awarded to Honeywell, Hughes, IBM, TRW, Texas Instruments, and Westinghouse for a three year development program ending in May 1984. A separate additional contract was awarded to Hughes Aircraft for the development of an electron beam lithography machine capable of patterning 0.5 micron circuits with a production rate that would be acceptable for large scale manufacturing. A major portion of this E-beam work was to be done by Perkin Elmer as a subcontractor.

The goal of Phase 1 was to develop the necessary processes, tools, and design environments for the production of 1.25 micron signal processing chip sets that would perform reliably in severe military environments, be affordable, and be usable in a wide variety of applications. This goal would support the key DoD objective of significantly reducing the delay in getting advanced semiconductor technology into fielded military systems.

The specific tasks to which the contractors were committed and the technical requirements associated with those tasks are contained in the contractual Statement of Work which is reproduced in Appendix IV. The tasks can be grouped into four principal areas and summarized as follows.

(1) Chip technology and fabrication

   o Develop a 1.25 micron baseline process to fabricate VHSIC circuits.
   o Establish a pilot production line to supply the projected number of VHSIC chips needed.
   o Supply chip packages which meet the military environmental conditions as well as the performance requirements such as speed, input/output connections, and power dissipation.

(2) Design, architecture, software, test (DAST)

   o Develop an architectural approach and design methodology which supports the VHSIC performance requirements.
   o Provide software development systems at a high order language level, preferably using Ada.
   o Include provisions for on-chip self test and fault tolerance at the chip or module level.

FIGURE II.2 — VHSIC PHASE 1 CHIP CHARACTERISTICS

Chip I.D.	Technology	Transistors (x1000)	Equiv. Gates (x1000)	On-Chip Memory	Size (Mils)	Power (watts)	I/O
Honeywell:PPP	ISL/CML	142	28	6K RAM	311x309	2.1	180
Sequencer	ISL/CML	136	27	80K ROM	300x300	1.8	180
Arithmetic Unit	ISL/CML	121	24	41K ROM	300x300	1.8	180
Hughes: Correlator	CMOS/SOS	72	18		368x315	0.7	148
Encoder/Decoder	CMOS/SOS	78	20		397x367	0.5	148
Signal Tracking Sys	CMOS/SOS	57	14		360x360	0.7	148
IBM: Complex Mult/Add	NMOS	88	37	None	320x320	3.3	240
Signal Proc Element	NMOS	20	8	None	157x157	0.7	144
T.I.: Data Proc Unit	STL		16	113K ROM	350x350	2.4	84
Vector Arith Logic Unit	STL		17	8K ROM	353x365	2.4	164
Vector Addr Generator	STL		11	64K ROM	301x312	2.2	84
Array Controller/Seq	STL		10	64K ROM	301x312	2.0	84
Device Interface Unit	STL		16	113K ROM	350x350	2.4	84
Multipath Switch	STL		4	None	250x265	1.8	84
General Buffer Unit	STL		10	64K ROM	301x312	1.8	84
Static RAM	NMOS	465		72K RAM	240x264	.45/.06	32
TRW: Window Addressable Mem	3D Bipolar	58	11		310x290	4.4	132
Content Addressable Mem	3D Bipolar	66	12		314x272	4.5	132
Register Arith Logic Unit	3D Bipolar	41	6		337x330	3.8	132
Multiply/Accumulate	3D Bipolar	42	8		320x298	4.1	132
Address Generator	3D Bipolar	34	10		336x285	4.0	132
Microcontroller	3D Bipolar	25	6		346x306	3.0	132
Matrix Switch	3D Bipolar	13	2		200x200	2.6	132
Four Port Memory	CMOS	60	13	4K RAM	290x313	0.3	132
Westinghouse: Static RAM	CMOS	400	100	64K RAM	190x310	0.54	42
Pipeline Arithm Unit	CMOS	133	33	1K RAM	340x350	0.7	224
Extended Arithm Unit	CMOS	100	26	.5K RAM	340x350	0.41	224
Extended Arithm Unit Mult	CMOS	92	23	2K ROM	340x350	0.37	224
Gen Purpose Controller	CMOS	79	20	8K ROM/.5K RAM	340x350	0.65	224
10K Gate Array	CMOS	40	10	None	280x304	0.45	224

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Honeywell - Solid State Electronics Division

Honeywell proposed to develop a 1.25 micron bipolar transistor IC technology as an extension of a 3.0 micron production process. This new process used a semicustom design approach based on the development of complex functional building blocks (macrocells) and supported by an integrated computer aided design (CAD) system that was assembled from a number of in-house and commercial CAD tools. The chip set proposed included a parallel pipeline processor (PPP), a sequencer, and an arithmetic chip. The Honeywell CAD system was demonstrated to tri-Service personnel in May 1984.

The 1.25 micron bipolar process used integrated Schottky logic transistor technology to provide high density random logic, random access memory, and read only memory on a single chip. The chip package, jointly developed by Honeywell and the 3M Corporation, was based on a ceramic package with 240 pin grid array I/O connections.

The first fully functional sequencer chip was fabricated in early 1984. The more complex PPP chip was fabricated by late 1984 and by the end of 1984 all three chips had been successfully fabricated. Motorola was subcontracted by Honeywell as a second source for chip fabrication. Motorola has successfully processed the Honeywell test chips, meeting all process control acceptance specifications.

An electro-optic signal processor (EOSP) brassboard was designed to demonstrate the operational improvements to be gained by using the VHSIC chip set. In July 1985, the EOSP brassboard successfully demonstrated the signal processing of the image for target area identification using the infrared image of a mock battlefield. The self test and fault tolerant features of the chip set were also demonstrated by operating the brassboard with three of the four installed PPP chips after one of the four was disconnected to simulate a failure.

Beginning in July 1985, the 1.25 micron pilot line was transferred from Minneapolis to Colorado Springs where a large new production facility had been built and equipped. The transfer process was substantially completed in 1986 and all subsequent Phase 1 production will be done there.

In 1986, Honeywell began a redesign of the EOSP chip set using current mode logic (CML) device technology and a standard cell circuit design approach. The redesign was undertaken to make the chip set serve a wider range of applications. Programming for specific applications is provide by an off-chip ROM while the chip set itself performs the more generic signal processing functions. The new designs permit the EOSP functions to be carried out with only two chips (a controller and the PPP). This redesigned EOSP chip set is expected to be 4-5 times faster than the original EOSP chip set demonstrated in 1985. Honeywell plans to complete the fabrication of the redesigned EOSP chip set in 1987. Progress details for this program are reported in references II.1 - II.8.

Hughes Aircraft

Hughes Aircraft proposed the development of three 1.25 micron CMOS/SOS chips for application in anti-jam communications systems. The devices consisted of a digital correlator, an encoder/decoder, and a signal tracking subsystem (STS). CAD system design tools for logic design, physical design, and verification were also included in the development program.

By the end of 1985, Hughes had successfully fabricated the first digital correlator and had designed a second version specifically to increase wafer processing yields. An initial design of the encoder/decoder was completed but effort on the redesign was terminated. The design of the third Phase 1 chip, the STS, was completed in mid-1985 and debugging continued through 1985. Both RCA and Rockwell were contracted as second sources for the correlator chip and both have successfully fabricated it. The Hercules CAD system was developed for use in chip design and verification. The system was delivered in August 1984 and is available to all DoD contractors from the Army VHSIC Program Office at Fort Monmouth.

In 1986, Hughes successfully demonstrated VHSIC chips operating in two related applications. The first demonstration was for a programmable modem in which five digital correlator chips were operated in parallel at 52 MHz to perform preamble correlation (detection of an arriving message) of the received waveform. The second demonstration used four digital correlators operating in parallel at the PLRS system waveform modulation rate of 20 MHz. These chips also demonstrated backwards compatibility by performing preamble correlation on the original PLRS waveform.

In July 1986, the encoder/decoder chip was redesigned and successfully fabricated by AT&T under a subcontract.

Early in 1986, the cause of non-functioning of the STS chip, the last chip of the original communications chip set, was diagnosed. A corrected chip design was prepared in two days and fabricated in only four weeks to yield fully functioning chips.

A family of 1.25 micron CMOS configurable gate arrays developed by Hughes was added to the Phase 1 contract in 1986. The design station CAD software to personalize these chips for prototype systems will be installed at ET&DL, Fort Monmouth, N.J., in early 1987. Details of the Hughes Aircraft Phase 1 program are reported in references II.9 - II.14.

IBM - Federal Systems Division

The 1.25 micron NMOS fabrication process proposed by IBM was an extension of an existing NMOS technology in use by IBM at Burlington, Vermont. This technology was transferred to the pilot line at Manassas, Virginia, and used for fabricating a single chip design which performed a complex multiply and accumulate function (CMAC). The chip contains logic for manufacturing test and on-line functional test. Four parallel arithmetic channels can be reconfigured by software

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to provide fault tolerance. IBM used a ceramic chip carrier with polyimide copper interconnects in a 240 pin grid array package.

The chip design is based on a master image architecture which combines a gate array image with a comprehensive set of custom primitives and macrocells that can be superimposed on the array.

The IBM brassboard was chosen to demonstrate a high performance acoustic preprocessor which significantly improved detection and expanded the capacity of the AN/UYS-1 ASW system. The system is designed for operational use in the P3, S3, and LAMPS platforms.

Design of the chip and package was completed by January 1983. The chip design contains greater than 35,000 gates with parameters as shown in Figure II.2. By December 1983 a CMAC had been fabricated, tested, and found to be fully functional. Independently, IBM developed a signal processing element (SPE) chip which is equivalent in performance to one quarter of a CMAC. Fully functional chips were obtained by December 1983. On May 1, 1984 IBM successfully demonstrated the acoustic signal processor brassboard.

Details of the IBM Phase 1 program are documented in references II.15 – II.20.

Texas Instruments

Texas Instruments proposed the development of eight multipurpose chips for programmable data and signal processing. These eight chips are listed in Figure II.2.

The seven logic devices are fabricated with bipolar Schottky Transistor Logic (STL). The memory uses NMOS process technology. Each logic chip has extensive on-chip test, including a four pin maintenance interface with scan in, scan out capability plus pattern generation and signature analysis, and on-chip diagnostics. The development included a 32 pad leadless ceramic chip carrier (LCCC) package for the SRAM, a 164 pad package for the VALU, and an 84 pad package for the remaining devices.

By the end of 1985, Texas Instruments had completed the design of seven of the eight devices and demonstrated their functionality in laboratory evaluation brassboards. The eighth unit, the GBU chip, was successfully fabricated in 1986.

The chip set was used in the design of a 1750A data processing module and a programmable array processing module to demonstrate signal processing for the Multimode Fire and Forget (M^2F^2) missile. The ICs were demonstrated by transferring data between two VHSIC 1750A evaluation computers. In July 1986, the 1750A evaluation computer was taken to the USAF/ASD System Engineering Avionics Facility (SEAFAC) to execute the MIL-STD-1750A Verification Software (VSW) suite resulting in full certification as a MIL-STD-1750A/Notice 1 computer. This is the first single chip CPU to receive this certification.

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In May 1986, the first VHSIC devices were delivered to Texas Instruments insertion programs. Since then, more than 1000 devices, including all eight chip types, have been delivered. Sample devices, primarily 1750A DPUs and SRAMs, were provided to other DoD contractors. In September, the ICNIA technology insertion program had demonstrated the functionality of a high density packaged 1750A computer module using VHSIC devices.

Fabrication yields of the VHSIC devices and the time to process wafers through the line improved significantly in 1986 allowing significant progress on analysis, correction, and validation of voltage and temperature range parametric yield/problems. As a result, design and process changes were implemented and full temperature (-55°C to +125°C case) and voltage (+/-10%) range parts were fabricated. The SRAM achieved the 25 MHz program performance goal. SRAM, MPS, and DPU chips were characterized so that production data sheets could be generated for initial sales of VHSIC parts.

Production of the SRAM, DPU, and MPS was announced in November 1986, and the other devices are expected to follow in 1987. Work will continue toward achievement of the full 25 MHz clock performance goal of each of the logic devices, primarily by reducing capacitance of the interconnects and transistors in the designs.

An additional chip will be added to the VHSIC family of processor parts. A 1750A Memory Management Unit, to extend 1750A memory addressing to 1 million words, will be fabricated in 1987. Details of the Texas Instruments Phase 1 efforts are contained in references II.21 - II.24.

TRW/Motorola

TRW proposed to utilize their existing 1.0 micron bipolar fabrication process for seven of the eight VHSIC chips listed in Figure II.2. The four port memory chip would be subcontracted to Motorola for design and fabrication using a 1.25 micron CMOS process developed by Motorola. Ceramic chip carriers with 132 pins would be used to package the chips.

Most of the CAD development was subcontracted to Sperry-Univac. It included four major development tasks: a hierarchical system language (HSL), a mixed level simulator, a multilevel data base, and conversion of existing CAD tools to the data base.

For the system brassboard, TRW proposed to design a generic high speed signal preprocessor for electronic warfare (EW) applications. The preprocessor was designed to take full advantage of the VHSIC chip capabilities to handle signal sorting, signal correlation, and threat warning in a very high signal density environment.

TRW produced a fully functional VHSIC chip - the matrix switch - in February 1983. The parameters of all eight TRW/Motorola chips are shown in Figure II.2. By July 1984, four of the chip types were tested as fully functional. By January 1985, all eight of the original chip family had been successfully fabricated.

In December 1984, a preliminary version of the brassboard was demonstrated to show:

o   the self test capability of the maintenance network, and

o   the major brassboard functions including the environmental filter, the histogrammer, and the signal processor.

A final EW brassboard demonstration and acceptance by the Navy took place on April 16, 1985. All eight types of the original TRW/Motorola VHSIC chips were used in the brassboard with a total VHSIC chip count of 57. The signal processing hardware was complete, the macrocode and macrocontroller were functioning correctly, all the signal processing functions were implemented, and operation in a complex emitter environments was demonstrated. The EW demonstration verified the VHSIC self-test capability, reduced weight, size and power consumption, and, through the use of advanced algorithms, operation in a high pulse density environment.

By December 1985, the TRW chip set was used to design, fabricate, and demonstrate an improved electronic subsystem for insertion into the AN/ALQ-131 electronic warfare pod. Details of the TRW/Motorola effort are contained in references II.25 - II.30.

Westinghouse/National Semiconductor

Westinghouse proposed to develop a 1.25 micron CMOS fabrication technology in cooperation with National Semiconductor. The family of chips included a 64K static RAM, a 10K gate array, three custom arithmetic processing chips, and a controller chip, as shown in Figure II.2. The chips were used to design a set of signal processing modules which would have wide applicability. CAD tools would be assembled into an integrated design system by Control Data Corp. Additional assistance in chip design and in CAD development was obtained from Harris Corporation and from Carnegie-Mellon University. The application brassboard was an airborne multimode radar processor.

The CMOS fabrication process was developed by National Semiconductor and installed in the pilot line located in Santa Clara, California. Three styles of leaded packages were developed having 42, 164, and 224 leads for memories, gate arrays, and custom logic chips, respectively.

The hierarchical chip design methodology was used to define the five custom chips (including memory) and nine personalizations of the 10K gate array. CAD tools were defined to support the entire process from the functional chip definition and architectural verification through electrical design, implementation, physical design, and verification.

During 1985, fully functional 64K static RAMs, 16K static RAMs, and 10K gate arrays were fabricated. During 1986, Westinghouse demonstrated a 1750A computer control function using 64K RAMs and an imbedded general purpose con-

troller chip.

An additional pilot line was established at the Westinghouse Advanced Techno-
logy Laboratory in Baltimore. Both the National Semiconductor and the Westing-
house facilities have fabricated personalized gate arrays for technology insertion
programs and plan to continue to produce VHSIC chips at both locations.

The National Semiconductor pilot line will emphasize fabrication of the
memories and gate arrays. Westinghouse will continue its pilot line operation
concentrating on the gate arrays. Further technical details on this program are
contained in references II.31 - II.36.

II.2 PHASE 1 - YIELD ENHANCEMENT

In order to demonstrate the advantages of VHSIC technology a substantial
supply of chips is needed for use in technology insertion projects. The goal of
the yield enhancement (YE) program is to ensure the supply and affordability of
the VHSIC chips by increasing the pilot line production yield and by introducing a
more disciplined production environment. Because of the new fabrication tech-
niques used in the VHSIC pilot lines and because of the developmental environ-
ment of these lines, the chips initially produced on the lines were all prohibitively
expensive for large scale use.

The yield enhancement program requires that the causes of low yield be iden-
tified and corrected. The task flow for this process is shown in Figure II.3.
Progress in achieving improved yield is measured by periodically starting the
fabrication of three consecutive lots of wafers that are collectively called a Yield
Verification Run (YVR). These YVRs are produced using the pilot line procedures
that are in effect at the time the run is started. Many additional lots are run
both to produce chips and to gather engineering data.

Each step in the manufacturing process has a yield associated with it. The
two yield numbers most often used are the overall yield of the production line
from wafer starts to packaged, tested chips at the output and the yield at "wafer
probe". Experience has shown that the yield for a given process increases as the
amount of product processed through the line increases. This is the "learning
curve" phenomenon normally encountered in all production line systems. There-
fore, a substantial amount of wafer processing is one of the requirements of the
YE program. Each contractor has a goal for the wafer probe yield and/or the
overall yield which the pilot line should achieve by the end of the program.

Figure II.4 is a summary of the latest yield results and includes the number of
VHSIC chips produced by each contractor.

Honeywell

The YE program at Honeywell began in 1985 with the objective of obtaining
10% packaged yield. The chip to be used for the yield measurements was the
sequencer.

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YIELD ENHANCEMENT PROGRAM

TASK FLOW

FIGURE II.3

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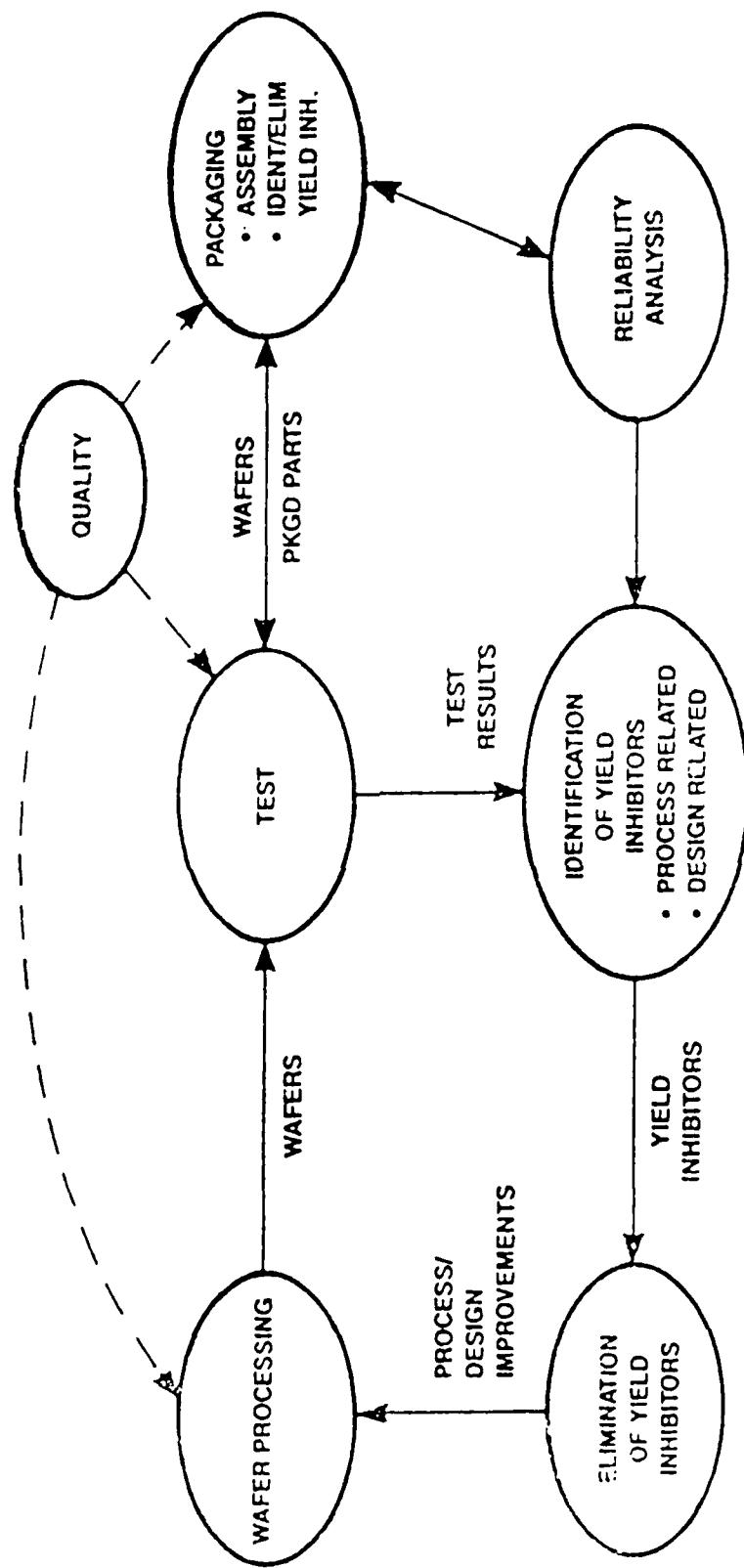
FIGURE 11.4 - VHSIC PHASE 1 CHIP YIELD AND AVAILABILITY STATUS (12/86)

COMPANY	CHIP		STATUS/CHANGES	MPY %	PRODUCED
Honeywell	Sequencer	FF	Being redesigned in CML to meet speed. Due 2Q/87	25	26
	Pipeline Prog Processor	FF	Being redesigned in CML to meet speed. Due 2Q/87	13	41
	Arithmetic Unit	FF	Being redesigned in CML to meet speed. Due 2Q/87	16	26
Hughes	Correlator	FF/S	Yield is for 3- and 4-section devices	7	823
	Encoder/decoder	FF/S	Redesigned and fabricated by AT&T	>15	>100
	Signal Trackg Subsys	FF/S		2	33
	20K Gate Array	FF/S	Logic error corrected 2/86	-	-
IBM	Complex Mult/Accum	FF/S		11	347
	Signal Proc'g Element	FF/S	NMOS in qualification. CMOS parts in mid-1987	34	>8300
T.I.	Static RAM (72K)	FF/S		83	76788
	Vector ALU	FF		7	34
	Vector Addr Gen	FF		27	1439
	Array Controller/Seq	FF		43	3786
	Data Processing Unit	FF		36	3316
	Multipath Switch	FF/S		41	1535
	General Buffer Unit	FF/S		19	302
TRW	Window Addr Memory	FF/S	TRW full line certification approx. 12/86	11	236
	Content Addr Memory	FF/S		10	170
	Matrix Switch	FF/S		62	502
	Register ALU		Brassboard functional to 22 MHz	20	535
	Multiply/Accum	FF	To 20 MHz	9	170
	Address Generator	FF/S		37	423
	Four Port Memory	FF/S	Motorola full line certification approx. 2/87	15	545
	Microcontroller	FF/S		15	426
Westinghouse:	Static RAM (64K)	FF/S	National Semicon pilot line certified 11/86	26	9000
	Static RAM (16K)	FF/S		78	41000
	10K Gate Array	FF/S	Personalizations underway	36	1200
	General Purp Contr.	-	Partially functional	-	-
	Extended Arith Unit	-	Partially functional	-	-
	Pipeline Arith Unit	FF/S		-	-

FF = logic is fully functional as designed; FF/S = Fully functional at 25 MHz or higher, at room temperature.
MPY = Best multiprobe yield at the wafer level averaged over at least one lot. Generally not at speed.

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By the end of 1985, the 1.25 micron bipolar line was processing test wafers for solving several identified yield inhibitors as well as verifying the utility of process simplifications. All the experiments were intended to improve the yield and reduce costs. New pilot line management procedures were instituted so that strict traceability of the VHSIC products would be available. During 1985, 114 lots were started in the pilot line. The best sequencer YVR lot during this period had a 14.1% probe yield. However, testing of the initial chips showed that they did not meet the VHSIC speed requirements and a redesign in CML would be required. This work was initiated under another program called EOSP Chip Productization.

In early 1986, several process improvements and simplifications were introduced, such as washed contacts to improve contact/junction quality and more selective metal etching. These changes contributed to process maturity, process simplification, yield improvements, and reduced costs.

The best probe yield achieved during the year for a full lot of each VHSIC chip type is shown in Figure II.4.

Overall packaged yield has improved to 2.1% against an interim goal of 3.4%. Most of the current yield loss is the result of damage to the surface of the chip during the evaporated solder bump process in packaging. This process has been changed to a plated bump process that is improving the assembly yield.

The new production line in Colorado Springs has fabricated fully functional sequencer chips on 6" wafers. Lot starts scheduled for the Minneapolis pilot line have been curtailed and the remaining runs are re-scheduled for the new production line. The last of the seven YVRs, using the CML design, is scheduled to be fabricated at Colorado Springs and be ready for test in June 1987.

Hughes Aircraft

The Hughes Yield Enhancement program is directed toward achieving an overall VHSIC packaged chip yield of 10% for the digital correlator chip. Four yield verification runs (YVR) were completed in 1985 which resulted in a functional wafer probe yield of from 1% to 3.1%.

During 1986, Hughes continued progress toward improving process yield. Although falling short to date of the yield enhancement goals, a functional wafer probe yield of 4.8% has been achieved.

During 1987, effort will continue to be directed toward improving yields. Additional effort will be directed at characterizing the various designs over temperature and voltage ranges. Process and/or design changes will be aimed at improving the device speed over the full temperature range.

IBM

IBM began work on a 27 month YE program in February 1984. The effort was applied to two Phase 1 NMOS chips - the SPE (signal processor element) and the CMAC (complex multiply accumulate).

Prior to 1986, IBM was achieving excellent processing yields for all parts run through its Manassas line with the exception of CMAC. Early in 1986, the company obtained over 40% probe yield on its SPE lots. At the same time, the CMAC probe yield was 0.6% an unexpected low value (based upon relative sizes).

The problems included forward and reverse bias failures and oxide leakage. Corrective actions were undertaken, including probing, laser isolation of failure sites, and modeling of the CMAC vs. the SPE.

The key problems were metalization defects and polysilicide to substrate leakage. It was suspected that the DC sputter cleaning step used on the CMAC was causing at least some of the problem. To check this out, two lots were run without the suspected sputter cleaning step. Probe yields of 8% and 6.9% confirmed this as a problem area. A new baseline process was transferred from Yorktown Heights to Manassas . Further investigation and continued process optimization is anticipated.

By the end of May 1986, 347 packaged CMAC chips had been produced. The best YVR lot of CMAC chips had a wafer probe yield of 8% while the best non-YVR lot was as high as 11%.

Twelve YVR lots of the SPE resulted in more than 8300 "all good" chips by August 1986. The average wafer probe yield for all SPE chips was over 20% One YVR lot reached a probe yield of 41.6%. The program was completed in August 1986.

Texas Instruments

The objective of the T.I. YE program is an overall package part yield of 10%. Since the yield is a function of chip size and processing complexity, the goals for wafer probe yield range from 39% for the SRAM to 4.5% for the DPU (1750A).

During 1985, the program emphasis was focused in two main areas. The first of these was the improvement of the front end process steps through particle reduction and equipment/process improvement efforts. The second major effort during the first half of this program was directed at isolating the principal causes for yield loss for both the NMOS SRAM and the bipolar STL designs. For the SRAM the main yield loss was by single bit failures thought to be caused by random defects.

The key yield loss factors identified for the STL designs were the lack of control of the Schottky diodes and the high defect level in the epitaxial silicon resulting in collector-to-emitter shorts. These problems have been eliminated by improving the processing procedures. The remaining major yield inhibitors associated with the inability of the STL design to operate over the required

voltage ranges. During 1986, recent design changes have demonstrated operation over a +/-20% voltage range and similar design changes are underway for the remaining STL designs.

As a result of the process and design improvements, the wafer probe yield has reached the values shown in Figure II.4. These results have surpassed the yield goals for each of the chip designs.

During 1987, the effort will continue to be directed toward improving the yields and characterizing the various designs over temperature and voltage ranges. Process and design changes will be aimed at improving the device speed over the full temperature range.

TRW/Motorola

The TRW YE program included two separate yield enhancement efforts - one for the TRW bipolar pilot line and one for the Motorola CMOS pilot line. The CAM and 4-Port memory (4PM) designs were designated as Yield Verification Run (YVR) vehicles at TRW and Motorola, respectively.

TRW

The TRW program began in 1984 on the company's VHSIC line at Redondo Beach. Part of the effort was later transferred to a facility in La Jolla as a backup to avoid interruption during a planned transfer of all TRW VHSIC work to a new pilot line at Redondo Beach. In the spring of 1984, a problem with the deposition of metal occurred with the CAM chip. Controls on the process parameters were instituted in order to correct this.

By May 1984, four fully functional Phase 1 chip types had been fabricated and were being included in yield enhancement runs - the MS, CAM, WAM and 4PM. At the same time, the first YVR of the CAM was processed.

TRW processed 960 wafers through the pilot line in 1985 and achieved defect densities as low 2.5/cm². A mask pellicle study was completed and the last two chip designs were fabricated successfully on first pass through the line.

The TRW yield enhancement effort ended in March 1986. The latest probe yield results for all of the bipolar chips is shown in Figure II.4.

Motorola

The Motorola YE program on the 4PM chip began officially at the MICARL facility in Mesa, Arizona in September 1984. The program was a 24 month effort scheduled to end in September 1986, with the final report to be delivered by the end of October 1986. The schedule has been relaxed to allow some final lots to be run and additional YE refinements to be made. Before beginning the program, Motorola redesigned the 4PM from a single level of polysilicide metalization to a two level refractory metal design to improve both speed and yield.

By the end of 1984, the major yield inhibitors were specifically identified as particles (foreign material) that affect almost all major operations and scratches due to material handling. During 1985 the following steps were taken to resolve these problems:

o particle count monitors were installed on all processing steps subsequent to and including polysilicon deposition. Material was processed only when the particle counts were judged to be low enough to result in a useful yield.

o wafer vacuum pickups were installed to replace tweezers. Other wafer handling and transport disciplines were introduced.

In addition to the process improvements, a number of design changes were incorporated into a new mask set in order to get higher performance, particularly speed. During the first half of 1986, five lots of 4PM chips, using the new mask set, have been processed at an average of 5.6% probe yield, with one lot as high as 8.4%.

Over 1220 wafers have been started through the pilot line. During this time improvements have been made in optical lithography and control of polysilicon critical dimensions. By September 1986, the probe yield of the 4PM had reached 15% and specifications and control limits were established for all critical process operations and installed in the data base.

Westinghouse Electric Corp.

At the end of the Phase 1 technology development efforts the VHSIC pilot line at National Semiconductor was successfully fabricating an 8K SRAM and a CAVP personalization of the 10K gate array using the 1.25 micron CMOS process. By instituting cleanliness improvements and more stringent process controls fully functional 64K SRAMs were produced in late 1984.

The yield enhancement program was then begun in February 1985. Test structures as large as the VHSIC chip itself were processed in the line to more clearly identify the yield limiting defects. At the end of 1985 probe yields of 10% on the 64K SRAM were being achieved. The most serious yield inhibitors were identified and process controls were explored.

In 1986, continued improvements were made in process control, maintenance management, and quality assurance. The process has achieved increased uniformity and control. New techniques for photomask protection and checking introduced in late 1985 resulted in first pass success for new chips designed for insertion programs.

To date, in the yield enhancement program, Westinghouse and National Semiconductor have processed over 300 VHSIC product lots of 20 wafers each. Over 41,000 16K SRAMs, 9000 64K SRAMs, and 425 crossbar gate arrays, all fully functional, have been produced. In addition, more than 1200 gate arrays of five different designs have been fabricated for insertion programs. The probe yield of the 64K SRAM has increased from an initial value of 0.6% to as high as 26%. The YE program ended officially in November 1986.

II.3 MILITARY QUALIFICATION

The goal of the qualification portion of the VHSIC program is to promote the insertion of Phase 1 VHSIC chips by demonstrating that they can be produced on certified production lines to meet performance specifications and JAN military reliability standards. A VHSIC Qualification Committee was formed early in the Phase 1 program to coordinate the JAN qualification requirements and proposed changes to those requirements. The committee has undertaken a three part program of activities.

Part I is a short term approach to qualify at least one VHSIC chip on each of the VHSIC pilot lines. This (together with the Yield Enhancement program) assures the users of these devices – the systems producers – of a supply of chips with a known, uniform level of performance and reliability. The qualification process consists of a sequence of definite procedures:

o   certification of the manufacturing facility (fabrication, assembly, and test procedures) in accordance with MIL-STD-976 and maintenance of the facility and procedures according to the specification,

o   testing of specified production lots in accordance with MIL-M-38510 and MIL-STD-883,

o   preparation and acceptance by the Government of a complete specification/- "slash" sheet for each qualified part type, and

o   periodic verification of the chip qualification by testing sample lots.

The qualification procedures are administered by the Defense Electronic Support Center (DESC) which performs the necessary audits of the facility, reviews the specification/slash sheets, and supervises the qualification tests. Changes to the standard test procedures will be incorporated as appropriate in MIL-STD-883 and made applicable to all VHSIC class ICs.

During 1984, plans for qualification of VHSIC devices were submitted by all the Phase 1 contractors. During 1985, they began work toward qualifying one or more chips by conducting chip electrical characterization programs and self audits of the pilot lines. Draft chip specifications were submitted to DESC by National Semiconductor for the 16K SRAM and by Motorola for the four port memory. DESC has conducted audits or pre-audits of the pilot lines at most of the VHSIC contractors.

The current status of Part I certification and qualification activities is summarized in Figures II.5 and II.6 and discussed individually below.

Part II of the program is a long term approach to qualification in which a set of generic qualification procedures for VHSIC class devices will be developed. The reason for adopting such an approach is that chips of VHSIC size, com-

FIGURE II.5 - VHSIC PILOT LINE CERTIFICATION STATUS

| COMPANY | SITE | PRE-AUDIT | | AUDIT | | CERTIFICATION |
		FEOL[1]	BEOL[2]	FEOL	BEOL	
Honeywell	Colorado Springs	1/87	7/87	7/87	9/87	9/87
Hughes	Newport Beach, CA			11/87	1/88	2/88
IBM	Manassas, VA		7/86	7/86	10/86	12/86
Motorola	Mesa, AZ	11/85	11/85	6/86	1/87	2/87
National Semiconductor	Santa Clara, CA Tucson, AZ			9/85		11/86 1/87
Texas Instruments	Dallas, TX (NMOS) Dallas, TX (STL)			2/87	3/87	6/87 3/88
TRW	Redondo Beach, CA San Diego, CA	8/85	8/85	11/86	11/86	1/87 1/87
Westinghouse	Baltimore, MD	9/87	9/87			11/87

1 FEOL = Front End Of The Line
2 BEOL = Back End Of The Line

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FIGURE II.6 - <u>VHSIC CHIP QUALIFICATION STATUS</u>

COMPANY	CHIP	TECHNOLOGY	SPECIFICATION PRELIMINARY	FINAL	PLANNED QPL[1]
Honeywell	PPP	Bipolar CML			12/87
Hughes	Gate Array	CMOS	8/87	9/87	1/89
IBM	SPE	NMOS	8/86		10/87
Motorola	4 Port SRAM	CMOS	10/85		7/87
National Semiconductor	64K SRAM	CMOS	4/86	11/86	9/87
Texas Instruments	72K SRAM	NMOS	11/86	5/87	3/88
	MPS	Bipolar STL	11/86	7/87	12/88
TRW	AG	Bipolar 3D	8/86		11/87
Westinghouse	Gate Array	CMOS	3/87	12/87	4/88

1 QPL = Qualified Products List

plexity, and cost can no longer be fully inspected and tested in the same way as previous generations of smaller IC chips. The generic approach takes advantage of test areas on the VHSIC chip, separate test chips, and separate test wafers to control and document the extremely complex fabrication process. These test structures , which must be used during the fabrication process, can also be used to provide information for certifying the quality of the line and for monitoring the performance of the chips produced.

The generic approach is expected to result in the same or even increased levels of reliability while keeping the cost and time required to qualify them to a minimum. The revised, generic criteria are expected to ease the following problems:

o   maintaining line certification as process changes occur,

o   qualifying new VHSIC chips as new/improved designs evolve, and

o   supporting VHSIC technology insertion.

A contract was awarded in September 1986 to a GE/AT&T team to develop the revised JAN qualification procedures and requirements. GTE was also contracted in August 1986 to focus specifically on the generic qualification problems for gate arrays. A joint DoD/Industry group has been formed to encourage broad participation in and awareness of the changes being made.

Part III of the qualification program will provide the improved test methods, reliability prediction models, and software tools needed for the qualification of VHSIC class devices. Test methods are being developed for the new packaging materials and techniques. The microcircuit reliability prediction methods and models are being revised to use design and process parameters measured on test chips. A tester independent support software system (TISSS) is being developed to use computer aided engineering tools for generating device specifications and test programs directly from CAD data. Under a TISSS contract awarded to the Harris Corporation, a preliminary design effort has been completed and further development is continuing.

In order to coordinate information on the DoD VHSIC qualification program with potential users, two VHSIC Qualification Workshops were held: the first in September 1985 and the second in September 1986. See references II.37 and II.38.

In summary, during 1986 the programs and efforts needed to begin the process of certifying the VHSIC production lines and qualifying the VHSIC chips to JAN specifications were put in place. The result will be that by the end of 1987 seven VHSIC chips will have been fully qualified. The changes in procedures and test methods needed to handle this new generation of IC technology are under development now and will be available as full scale production evolves. Appendix II contains a listing of the various qualification contract efforts under Phase 3-Current Projects: Reliability/Testing.

Honeywell

A contract for qualification of the PPP chip and certification of the 6-inch wafer pilot line at Colorado Springs was awarded in October 1986. The line is scheduled to be certified by September 1987 and the chip to be qualified by December 1987.

The chip to be qualified will be the PPP which has been redesigned from ISL technology to CML technology in order to meet the 25 MHz speed requirements. The PPP chip will be assembled in a hermetic pin grid array package using a tape automated bonding (TAB) approach. Screening procedures for the TAB interconnect system will be developed jointly by RADC and Honeywell.

Hughes Aircraft

Hughes has elected not to qualify any CMOS/SOS VHSIC products at present. Instead, it proposes to demonstrate the ability to produce and qualify a VHSIC bulk CMOS gate array in accordance with the generic qualification procedures being developed in Part II of the qualification program. Hughes plans to complete characterization of a test circuit by June 1987 and a macro test chip set by July 1987. Line certification by DESC is expected in February 1988 and complete qualification of the gate array in January 1989.

IBM

IBM first proposed an approach called "qualification by observables" which relies on test structure measurements to predict the control of the pilot line and the quality of devices. This approach would be compatible with "generic qualification" but was not accepted for current DoD qualification requirements.

A contract for the qualification of the NMOS SPE chip in a hermetic flip-chip package to current JAN requirements was awarded in November 1986. DESC conducted a preliminary audit of the IBM VHSIC NMOS pilot line at Federal Systems Division in July 1986. Audit of the flip-chip mounting and assembly processes took place in October 1986. DESC issued a Letter of Certification for the full VHSIC process in December 1986.

An initial draft device specification was submitted to DESC in August 1986 and is being circulated for coordination. Completion of qualification of the SPE is expected in October 1987.

Texas Instruments

Texas Instruments began a 12-month program on the characterization of two chip types in April 1986. The two device types chosen were the 72K static RAM, representing the NMOS technology, and the multipath switch, representing the bipolar STL technology. Both chips are packaged in leadless chip carriers.

The characterization program consists of two phases:

o   development of draft quality/reliability and electrical specifications for the SRAM and MPS and then demonstration that the chips meet these specifications,

o   screening and qualification testing of the SRAM and MPS in accordance with MIL-STD-883, Methods 5004 and 5005, and the final device specifications.

The first phase of this program is nearly complete, with four self-audits completed and a final self-audit of the VHSIC manufacturing facility scheduled in the fourth quarter of 1986.

Draft device specifications are being prepared and five lots of SRAM and MPS chips are currently being characterized electrically. The reliability/screening procedures will be demonstrated with the above devices in April 1987. T.I. has submitted a plan to continue its initial program to qualify the 72K SRAM. Certification of the line by DESC is scheduled for March 1987, with complete qualification and QPL listing by March 1988. Either the MPS or the DPU, processed with STL technology, is projected to be qualified by the end of 1988.

TRW/Motorola

TRW and Motorola began work on the certification of their VHSIC fabrication lines in 1985. The chips to be qualified are the address generator (AG) and the four port memory (4PM). DESC conducted a pre-audit of the TRW bipolar fabrication line and assembly/test facilities (in Redondo Beach) in August 1985. A DESC pre-audit of the Motorola fabrication line and the assembly and test area in Mesa took place in November 1985.

TRW has shifted the wafer fabrication from Redondo Beach to the LSI Products Division in San Diego. Assembly and test will remain in Redondo Beach.

A contract was awarded to TRW in July 1986 for the JAN qualification of the AG and the 4PM. An initial draft device specification for the AG was submitted to DESC in August 1986 and is being circulated for coordination. A final DESC audit was conducted in November 1986. Full line certification is expected in January 1987. QPL listing of the AG is expected by November 1987.

An initial draft specification for the 4PM was submitted to DESC in October 1985. An audit of the Motorola fabrication line was conducted in June 1986; audit of the assembly area is scheduled for January 1987. Certification of the line is expected by February 1987. Completion of qualification and QPL listing is expected by July 1987.

Westinghouse/National Semiconductor

A contract was awarded in October 1986 to Westinghouse for qualification of the 64K CMOS SRAM on the National Semiconductor pilot line in Santa Clara. The fabrication line was audited in 1985 and certified in February 1986 for the

production of 16K SRAMs and in November 1986 for 64K SRAMs.

After circulation of the official initial draft specification for the 64K SRAM, the final draft was issued in November 1986. Completion of the qualification of the 64K SRAM is expected by September 1987.

Westinghouse has proposed to certify a CMOS line at the Baltimore Advanced Technology Laboratory in November 1987 and then qualify a representative personalization of a VHSIC CMOS gate array by April 1988.

SECTION III

VHSIC TECHNOLOGY INSERTION

"Technology Insertion" is the term used to describe the use of any of the VHSIC products - hardware or software - in the development of a new system, in the redesign of an older one, or in the maintenance and improvement of an existing one. It constitutes one of the basic goals of the VHSIC program. Since it necessarily involves the linking of "high tech" with real life operational systems, it also constitutes one of the more difficult problems that confronts the VHSIC Program managers.

The wide spread use of VHSIC technology in military systems will have a profound impact on the process by which DOD acquires its weapon systems. New procedures must be implemented for the detailed specification of hardware and software components, the standards by which these components are tested and qualified for military use and the specification and control of the logistics pipeline from manufacturer to field depot to fielded system and back. A policy stance must be adopted which supports the advances in military capability offered by VHSIC Technology.

The development of a DOD directive for the use of state of the art/VHSIC technology in weapon systems has begun (see reference VI.10). Supporting high level statements have already been issued by the Army, Navy and Air Force. Each Service is preparing a VHSIC Technology Transition Plan in accordance with specific service needs. Draft versions of the Army, Navy and Air Force Transition plans have been prepared.

By 1988 it is expected that the actions taken during Parts I and II of the VHSIC chip qualification and availability plan will provide a sound basis for the orderly and routine application of Phase 1 VHSIC products to military systems. They will provide the framework for the introduction of newer Phase 2 VHSIC products scheduled to be available at that time.

As mentioned in Section I, the system program manager has a relatively fixed budget and time schedule within which he is committed to deliver his product. The situation forces him to be conservative in his choice of technology. On the other hand, the performance of the system usually can be optimized by using better technology. This encourages him to use the most advanced technology available.

Since VHSIC is a very new technology, a new approach to insertion had to be devised. The system program managers were hesitant to take the risks associated with a chip technology that was not in production, had not been qualified to military standards, existed only in small sample quantities, and was still expensive. A solution to these problems was developed by the VHSIC Program Office along three lines:

o undertake to cost share a limited number of pilot studies and hardware insertion projects in each of the Services,

VHSIC TECHNOLOGY INSERTION
AREAS OF GREATEST BENEFIT

RELIABILITY AND MAINTAINABILITY
- AN/ALQ-131
- ATE
- F-15 LRM CC
- F-16 PSP

TECHNOLOGY GROWTH DESIGNS
- PAVE SPRINTER
- AN/AYK-14

NEW CAPABILITY
- MEDFLI
- HF/EHF COMM
- LLGB
- ATR
- SPEECH PROCESSOR
- SPACE MIL-STD-1750A

PERFORMANCE ENHANCEMENTS
- PLRS
- FIREFINDER
- AN/UYS-1
- IRST
- TOW-3
- AN/APG-65
- E-3A PSP
- COMBAT DF
- F-15 RADAR RWR

SIZE/WEIGHT/POWER
- LHX
- HELLFIRE
- MK 50
- AOSP

ARCHITECTURE INNOVATIONS
- LHX
- CSP

LIFE CYCLE COST
- AUTOMATED TEST
- VHSIC 54XX TTL
- MIL-STD-1750A
- MILSTAR
- EMSP
- LOGISTICS R E

o   independently fund a yield enhancement effort added to the Phase 1 development. This effort would be designed to put the fabrication of VHSIC chips on a more manufacturable basis, increase the production yield, and hence decrease the unit cost of VHSIC products (see Section II.2),

o   initiate a qualification program to take a selected number of the VHSIC chips through the JAN qualification procedures which would place them on the Qualified Parts List and make them available for system use (see Section II.3).

In response to the VPO decision to fund technology insertion efforts in 1983, each of the Services submitted a number of systems as candidates for near term VHSIC insertion. From these candidate lists the systems to be funded for study and/or hardware development were selected on the basis of the following criteria:

o   significant quantitative, identifiable benefits such as improvements in weight, space, power, reliability, and functional performance,

o   a strong commitment from the system program office,

o   utilization of chip set architectures which had multiple applications,

o   early demonstration or use of VHSIC technology,

o   life cycle cost reduction,

o   participation of non-VHSIC contractors.

III.1   ARMY

From the original list of approximately 40 systems submitted by the Army in 1981, fifteen systems were designated as the strongest candidates for VHSIC technology insertion. The current systems into which VHSIC technology is being inserted are discussed below.

1. ENHANCED PLRS USER UNIT (EPUU)

In order to provide the improvements needed in the PJH system, Hughes Aircraft has defined a VHSIC chip set for insertion into the signal message processor module of the EPUU. Existing Hughes digital correlator chips packaged into hybrids are to be used but a new time domain algebraic encoder/decoder has been developed. Two gate array chips are also being designed to provide the I/O and "glue chip" functions.

A six month study for VHSIC technology insertion into the EPUU has been completed. The study identified potential improvement in the anti-jam and ECCM performance of the system while also providing increased reliability. Power and

weight would both be decreased by one half while the MTBF would increase by 25%. A hardware program was begun in September 1984 and two brassboards have been developed. The algebraic encoder/decoder chip was successfully redesigned and fabricated by AT&T in July 1986 under a subcontract to Hughes.

As the VHSIC components become available they will be integrated into the brassboard processors. The current plan is to procure 15 EPUUs with VHSIC chips in the signal message processor module. These EPUUs will be tested operationally in 1988. A VHSIC versus non-VHSIC PLRS unit production decision will be made in 1989 based on the test results.

Based on current design information, the use of VHSIC technology will result in a saving in procurement costs of $300 million plus an additional $300 million saving over the full life cycle of the system.

2. LIGHT HELICOPTER (LHX) COMPUTER

The projected production of over 4500 LHX aircraft provides an opportunity for very large scale application of Phase 1 chips. VHSIC technology can be used in two or more LHX processors each of which may contain more than 100 VHSIC chips. It would be impossible without the VHSIC technology to provide, within the weight and power constraints of the aircraft, the highly automated sensing and control environment needed for a one man crew to accomplish the entire mission.

Analyses to date have indicated that VHSIC Phase 1 devices are capable of the required performance. Each of five technology integration teams were assigned similar tasks in 1985 to design and validate an optimum LHX processor with VHSIC technology. The results of these five efforts will be used to direct the computer design and development program of the prime contractor during the full scale development phase of the LHX aircraft. Brassboard development is in progress.

Development and demonstration of a VHSIC processor will continue into 1987 and beyond. It is expected that a VHSIC processor will be incorporated into the full scale development program for the LHX which is scheduled to start in 1989.

3. TOW AUTOMATIC TARGET TRACKER

This effort will result in a VHSIC processor which will provide such increased system performance as higher probability of hit, improved rate of fire, and reduced gunner exposure to counterfire. The computer will perform both the present missile tracking function and a new automatic multiple target tracking function. The added computational and processing required to track multiple targets could not be packaged within the missile weight and size restrictions without VHSIC technology.

The breadboard VHSIC processor has been defined by Texas Instruments and Hughes Aircraft. The brassboard phase was awarded to T.I. Development of the hardware began in 1985 and will continue into 1987. Flight tests of the TOW automatic target tracker with the VHSIC brassboard are scheduled to begin in
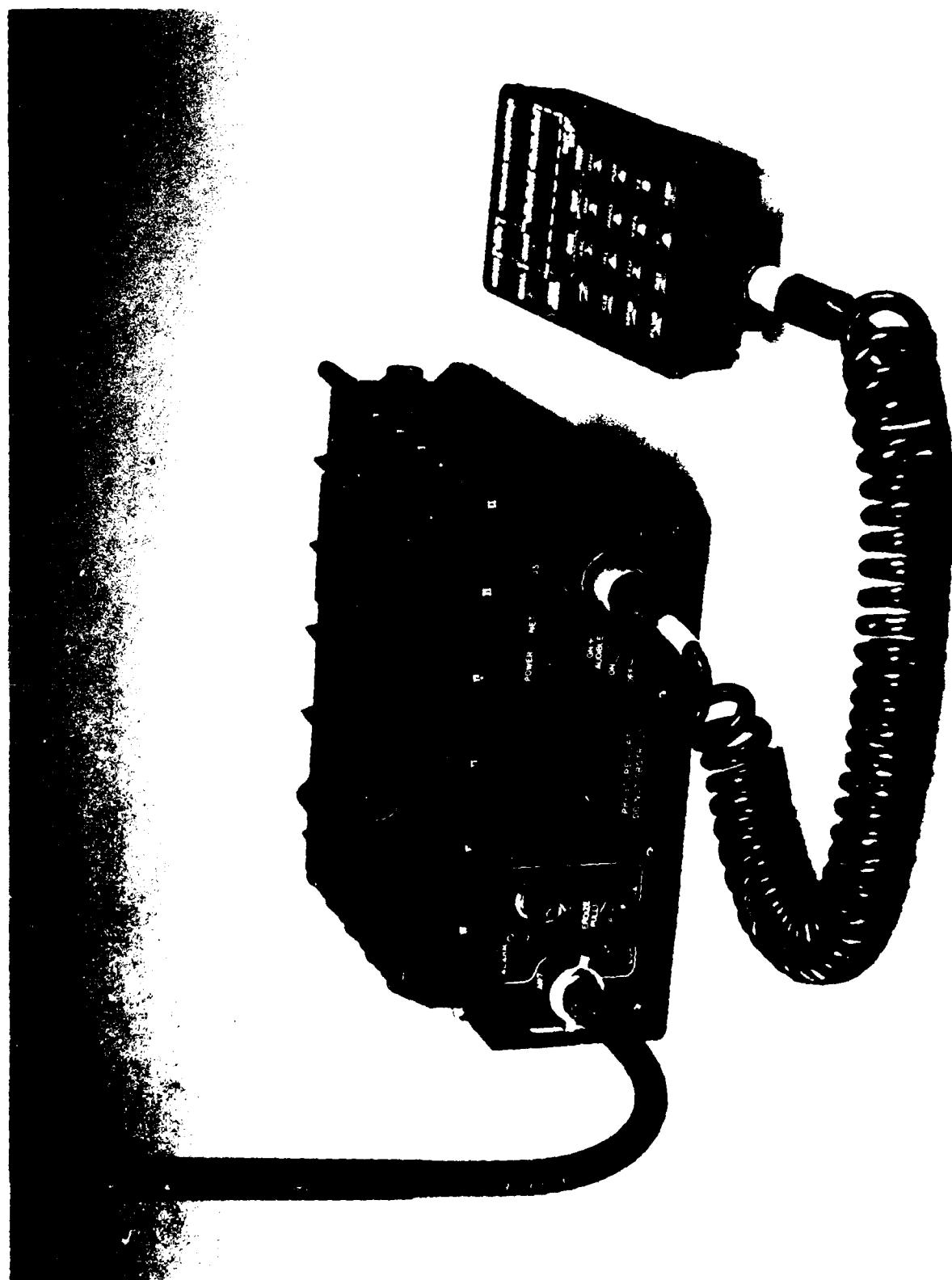
FIGURE III.2

EPLRS UNIT AND USER READOUT

1987.

4. TOW WIRELESS COMMAND LINK (WCL)

The objective of this program is to design and fabricate a Wireless Command Link (WCL) for the TOW missile. At present the TOW is limited in velocity and range by the wire guidance system. The VHSIC WCL will result in greater range, higher velocity, and simultaneous guidance of multiple missiles.

Breadboard characterization tests of the VHSIC WCL were successful. The WCL receiver design has been completed, and the receiver is now being fabricated. Some VHSIC chips have been designed and fabricated. More than 80 wafers, each containing 30 chips, have been processed. A chip dynamic test program has been completed. Several chips have been packaged, and dynamic testing of packaged chips is now going on.

The static tests of the WCL are being conducted using a modified TOW missile containing a WCL VHSIC receiver and the WCL breadboard transmitter. Future plans include modifying one TOW launcher (with a WCL transmitter) and 11 TOW missiles (with WCL receivers) and conducting dynamic flight test to validate the VHSIC design.

5. FIREFINDER RADARS

Use of VHSIC technology will significantly improve the performance of the FIREFINDER system in handling and classifying targets. At the same time, reducing the power by 60% and reducing the parts count will also make it possible to reduce the size of the FIREFINDER radar, increase system mobility, and increase its survivability. Reconfiguration of the radar on a single vehicle will reduce the crew required from 8 to 4 personnel for the AN/TPQ-36 radar and from 12 to 4 personnel for the AN/TPQ-37 radar. The result will be a projected saving of $857 million during the life cycle of the FIREFINDER radars – a sum that is almost equal to the total VHSIC program budget.

A system study and analysis has been completed in which (1) VHSIC processor architecture and chip requirements have been identified, (2) FIREFINDER system modifications have been defined, and (3) a plan has been prepared for the demonstration of this VHSIC technology insertion.

A brassboard model of the VHSIC processor is being developed and fabricated. It is anticipated that the brassboard model will be completed by the end of FY87. The brassboard VHSIC processor will then be integrated into an existing FIREFINDER radar, and a test demonstration will be conducted on the FIREFINDER test range with simulated target reaction signals within a normal jamming environment situation.

6. COMBAT VEHICLE VHSIC PROCESSOR

In addition to providing potential for future performance growth and reduced

system life cycle costs, utilization of VHSIC technology will reduce weight and size of the processor, increase computational throughput capacity, and improve performance of present combat systems. It is anticipated that a general VHSIC processor can be designed which is applicable to the following combat vehicle candidate systems:

o ABRAMS (M-1 Series) Tank   8000 systems
o BRADLEY Fighting Vehicle (M2/M3)   7000 systems
o M60A3 Tank   5400 systems
o HIP (Automatic Howitzer)   1700 systems

TOTAL   22,100 systems

Design of a VHSIC based processor (brassboard model) began in 1986, and long lead items for the processor were identified.

It is anticipated that fabrication of the brassboard model of the VHSIC based processor will be completed in 1987. This will be followed with a field demonstration of the brassboard processor in an M1A1 tank. The development prototype design should begin in 1988.

7. MINIATURIZED ELECTRONIC DIRECTION FINDING LOCATION INDICATOR (MEDFLI)

MEDFLI is a system designed for installation on a remotely piloted vehicle to locate and identify complex and dense electronic threats of the 1990s and beyond. VHSIC technology insertion in the electronic support measure (ESM) processor and the threat association module (TAM) will result in a 3 to 1 increase in processor throughput that is required for the MEDFLI system.

Contracts for the development of a VHSIC based ESM processor and TAM have been awarded, and development of these items using VHSIC Phase 1 chips is now underway.

Development of the ESM processor and TAM will continue through 1987. Engineering development of the VHSIC components and insertion of these components with the MEDFLI system will occur during the development phase of the MEDFLI program, starting in 1988.

8. HELLFIRE WEAPON SYSTEM - IMAGING INFRARED SEEKER

The IR Seeker provides a "fire and forget" capability for the HELLFIRE, an anti-armor weapon system using a semiactive laser guidance subsystem. VHSIC technology provides the increased data throughput required for the fire and forget feature without reducing the weight and space allocated to the warhead or other non-electronic functions.

Contracts were awarded in 1986 to two contractors for VHSIC development. One contractor was tasked to develop a prototype VHSIC Seeker and the second

contractor to develop a VHSIC based processor for integration into the HELLFIRE Seeker. VHSIC efforts will continue through 1987 into 1988.

The data, information, and technical knowledge/techniques learned in this effort will be applied to the FOG-M missile and is applicable to other missile systems.

III.2   NAVY

1. ENHANCED MODULAR SIGNAL PROCESSOR (EMSP)

In the FY83 Defense Authorization proceedings, Congress mandated that the EMSP development effort would be a VHSIC proof-of-principle insertion. The EMSP is the Navy's next generation standard signal processor, designated AN/-UYS-2. This system meets signal processing requirements through the 1990s for air, shore, and sea applications in sonar, radar, electronic surveillance, and communications systems. The AN/UYS-2 is constructed of Standard Electronic Modules (SEM) and is designed to be interoperable with other standard Navy computers and to be fully compatible with standard computer support programs. Life cycle supportability and ease of technology insertion are an integral part of system design.

AT&T is providing the system integration effort. Honeywell, as a subcontractor, is developing the chips needed to build the demonstration brassboard(s).

The VHSIC contribution to the EMSP is in the development, integration and testing of a floating point arithmetic unit (FPAU). This 32 bit floating point processor permits the utilization of new algorithms and processes data faster, more accurately, and more efficiently than present day processors while concurrently resulting in less expensive coding. Incorporation of advanced VHSIC functional elements into the EMSP provides the necessary throughput to handle expected increases in sensor array size.

The FPAU will use three VHSIC chip types: a floating point multiplier, a register arithmetic logic unit (RALU), and an SRAM. There are five chips per set and each machine will use dozens of chips. The chips range in complexity from 17,000 to 32,000 equivalent gates. Functional verification of the chip set and the breadboard assembly was completed in July 1986. Functional testing at speed took place in September 1986. Fifteen of the chip sets are currently being tested and five additional sets are scheduled for test in December 1986.

The first functional SEM boards are due in the first quarter of 1987; delivery of prototypes are scheduled to begin in the second quarter; laboratory development models of the SEM hardware will begin later in 1987. In April 1987, the interoperability and signal processing capabilities of the system will be demonstrated. A comprehensive performance analysis is expected to be completed by June 1987.

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2. MK-50 ADVANCED LIGHTWEIGHT TORPEDO (ALWT)

The MK-50 ALWT is the Navy's next generation torpedo designed to counter the continually evolving Soviet submarine threat. It will be the primary ASW weapon for air and surface platforms, as well as the principal submarine standoff weapon. Technical and operational evaluation of the Honeywell insertion program is scheduled for during 1987-88.

VHSIC insertion provides significant benefits to the MK-50 system: a saving of 5 inches in length and 40 pounds in weight which were needed in order to carry a larger warhead; increased reliability by having 1,300 fewer components and 15,000 fewer solder joints; increased capability for the embedded AN/AYK-14 computer (which is a separate VHSIC insertion program); power reduction of 16 watts; and 540 square inches less circuit board area. The overall result is a reduction in life cycle costs because of better reliability and maintenance characteristics with the same or better performance parameters.

VHSIC chips are being used in the digital receiver and in the command and control subsections. The TRW microcontroller chip, the TRW address generator chip, the T.I. SRAM, and a number of ETA/Honeywell gate array personalizations are being used. One receiver gate array is being designed and one is being fabricated. One gate array for the combined memory and bus controller section has been fabricated and tested while a second is expected to be complete in December 1986.

3. PROGRAMMABLE SIGNAL PROCESSOR (PSP) FOR THE AN/APG-65

The AN/APG-65 radar is a coherent multimode pulse doppler radar now operational in the F/A-18 aircraft. This radar provides long range air-to-air target detection, tracking, and special air combat maneuvering modes. In addition, fire control information for medium and short range missiles as well as for the 20 mm gun is provided.

The PSP can provide significant improvements in the performance of the radar by increasing the throughput and memory capacity twenty times, with a concurrent tenfold reduction in required power, weight, and volume. VHSIC enhancements would result in one tenth the parts count, resulting in a reduction in life cycle cost and a significant increase in reliability. Under a related program, the multimode guidance project, a guidance system for long range surface-to-air missiles is being developed.

This program has recently been halted due to funding constraints.

4. AN/AYK-14(V) STANDARD AIRBORNE COMPUTER

The AN/AYK-14(V) Standard Airborne Computer is a modularly designed general purpose digital computer that has been designated a Navy Standard Computer. This computer is functionally and physically partitioned into replaceable modules to provide operational flexibility. The AYK-14 is currently in use or

intended for use in major weapons systems such as the MK-50 ALWT, the E-2C, EA-6B, P-3C, F-14D, A-6F, EP-3E, AV-8B, F/A-18, SH-60B, and the automatic carrier landing system. Production quantities of 12,000 to 14,000 are expected by 1995.

Sperry and Control Data have each completed a 10 month study of all aspects of VHSIC insertion into the AN/AYK-14.

A 48 month contract to develop a VHSIC version of this computer was awarded to Control Data Corporation in February 1986. The VHSIC Processor Module (VPM) is expected to use one half as many major functional components, provide a threefold increase in processing capability, and maintain the current footprint. The reduction in components is expected to result in a tenfold increase in reliability to an MTBF of 15,000 hours.

The program will develop four standard cell VHSIC chips: a cache memory controller, an arithmetic unit, a bus controller, and an input/output chip. These chips are currently in the design/simulation phase.

5. HF/EHF COMMUNICATIONS TERMINAL

EHF/HF systems provide the minimum essential survivable communications systems. The Milstar EHF and the High Frequency/Anti-Jamming (HFAJ) programs will both be greatly enhanced by VHSIC technology insertion. HF and EHF terminal functions can both be incorporated into a single terminal by using VHSIC signal processing capabilities. At the same time, the terminal size and weight is reduced by 50%, the reliability is increased five times, and the system can be rapidly reconfigured for different signal environments. The cost savings and performance improvements are expected to have a major impact on system acquisition.

This program will provide a common brassboard for both the Navy and the Air Force. The electronic warfare brassboard and the MILSTAR brassboard being developed by TRW are being used as the basis for this new VHSIC Terminal brassboard (VTB). The EHF section of the VTB is common to the Navy and Air Force systems. The EW signal processor is used in both the VTB HFAJ section and the communication brassboard (see below). The TRW chips being used are the convolutional decoder, the FFT chip set, and the configurable gate array, all developed during Phase 1.

The convolutional decoder and the FFT arithmetic chip are completed. The FFT control chip is expected to be finished early in 1987. Fabrication of the first brassboard is scheduled for December 1986, with hardware/software integration in April 1987. Final delivery of four brassboards (two for the Navy and two for the Air Force) is expected in late 1987.

6. VHSIC COMMUNICATION BRASSBOARD (VCB)

This program will demonstrate a VHSIC communications signal processor packaged in Standard Electronic Modules (SEM) and a preprocessor using universal

matched filters. The signal processor being developed under this program is common to the TRW Phase 1 EW Processor brassboard, the HF/EHF Terminal brassboard and ICNIA. Navy and Air Force versions of this brassboard are to be delivered in 1987 (see above).

Aircraft require an HF communications processor/modem and controller operating in conjunction with current HF radios to provide the capability for HF ECCM and NTDS Link 11 improvements. The improvements can only be accomplished with VHSIC technology. The basic designs for the UMF and the signal processor form the basis for generating multiple SEM dual printed circuit card modules. These modules are compatible for use in the airborne processor/modem and controller equipment. Each of the modules makes extensive use of the TRW Phase 1 chips as well as other chips currently being developed.

A seven module VHSIC signal conditioner, common to the tri-Service ICNIA program, will process waveforms similar to HFAJ waveforms and provide pulse decoding of GPS and JTIDS signals. The brassboard is currently being fabricated for a scheduled delivery in early 1987.

7. ADVANCED ANTI-RADIATION MISSILE (ARM) SIGNAL PROCESSOR (AASP)

This project will apply VHSIC technology to the signal processor used in present and future anti-radiation missiles. The increased processing capability available with VHSIC is required to handle the threat signal environments of the 1990s.

An initial six month study was conducted by Texas Instruments in 1985 to recommend an appropriate VHSIC based low cost seeker. The study defined the signal processor architecture, VHSIC chips, and performance parameters. A procurement is underway for development and demonstration of a brassboard.

VHSIC benefits for the new system include a decrease in power, weight, and space requirements, along with substantial increases in the throughput and memory needed for future ARM applications. An estimated 25 percent cost reduction and 50 percent reliability improvement would be realized with VHSIC technology over comparable VLSI designs. Efforts are underway to fund this program in 1987.

8. VHSIC SIGNAL CONDITIONER (VSC)

The VSC has been developed by IBM as a replacement for the input signal conditioner (ISC) of the AN/UYS-1. The AN/UYS-1, designed primarily for airborne applications, is the Navy's most recently deployed acoustic signal processor. Since the next version of this processor, the EMSP, will not be in full production until the 1990s, product improvement to the AN/UYS-1 is necessary to match the signal environment that will be encountered throughout the remainder of its lifetime.

The ISC, one of four major subunits, provides an interface between the sonobuoy sensors and the digital processors. The ISC provides an analog interface to the ASW sonobuoy receiver, prefilters the analog data, performs the

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VHSIC

AIR ANTI-SUBMARINE WARFARE SYSTEM
(P3-C)

CP-901 TACTICAL COMPUTER

OPERATOR DISPLAYS/ENTRY

AN/UYS-1 ANALYZER UNIT

AN/USQ-78 DISPLAY CONTROL UNIT

DIGITAL MAGNETIC TAPE UNIT

VHSIC ACOUSTIC PREPROCESSOR BRASSBOARD

ACOUSTIC DISTRIBUTION BOX

RECEIVERS

ANTENNA

PLATFORM

SENSORS

ACOUSTIC SOURCE
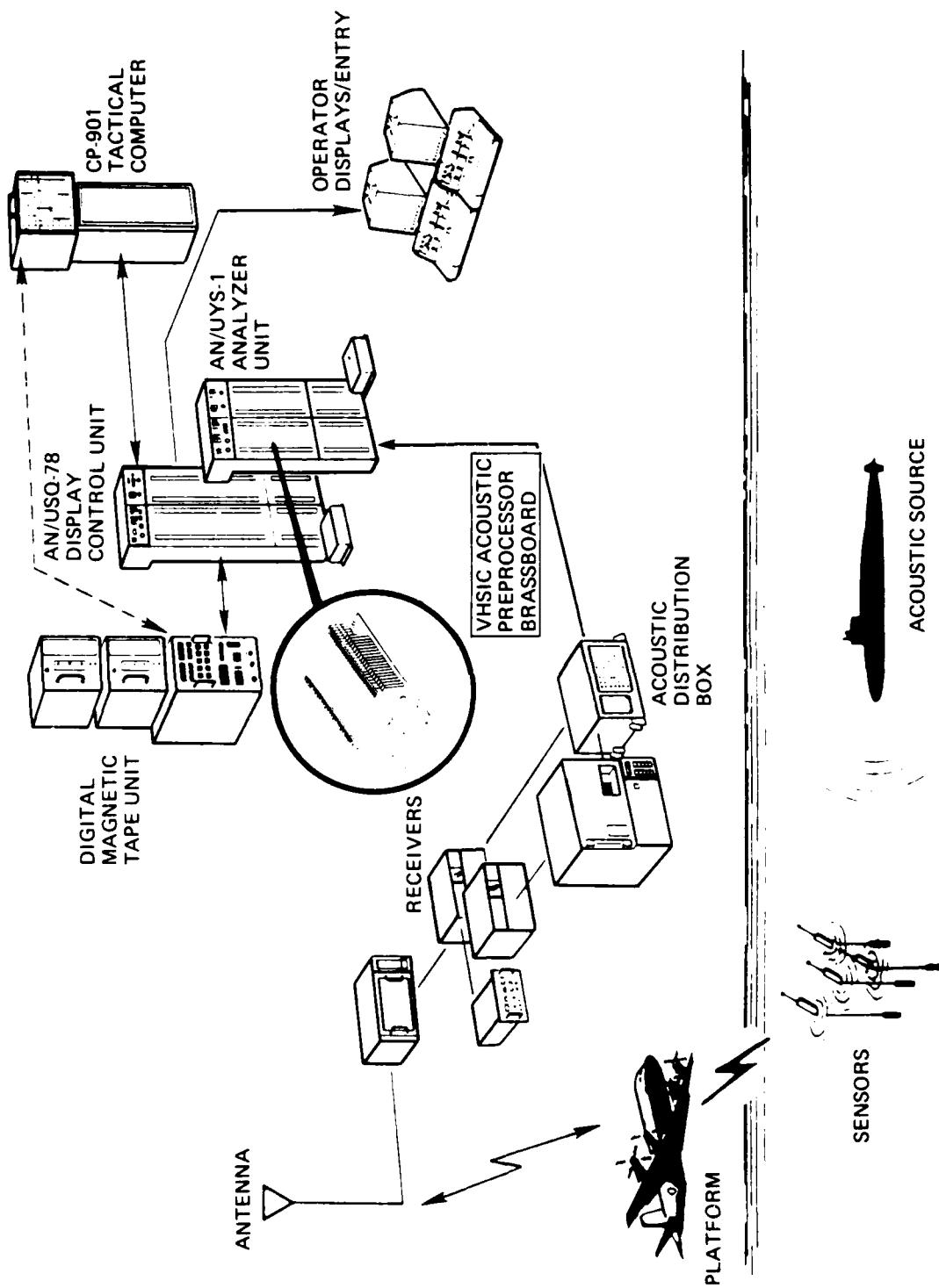
V0057-2

FIGURE III.3

analog-to-digital conversion, and presents the data in a format compatible with other subunits.

The VSC replaces the ISC with a version based on the IBM Phase 1 brassboard which uses the complex multiply and accumulate (CMAC) chip. The VSC provides a new front-end processor architecture with high speed processing capability and doubles the number of sonobuoy channels that can be processed.

It has been demonstrated that the VSC, which has the same footprint as the ISC, can be installed by a technician in under 30 minutes. Insertion and operational demonstrations were conducted in August 1986 at the Naval Air Development Center and a month later at Andrews Air Force Base. These demonstrations proved the ease of installation and the enhanced signal processing capability provided by the VSC.

9. COMBAT DIRECTION FINDER

This program is based on a Sanders Associates IR&D study which demonstrated a vector product calculator with 100 MOPS throughput. The calculator uses Phase 1 chips from IBM, TRW, TI, and Motorola. This application of VHSIC chips reduces the time required to compute groundwave and skywave line-of-bearings by at least two orders of magnitude. The calculator has been breadboarded and is currently under test. Brassboard demonstration is scheduled for February 1987. Construction of an advanced development model is expected to begin early in 1987.

10. MODULAR VHSIC PROCESSOR FOR ATA AND FUTURE NAVAL A/C

This 1986 new start program will investigate and demonstrate the application of VHSIC to modular hardware in future Navy aircraft employing distributed architecture systems. By extensive use of existing VHSIC chips and hardware, significant reductions in weight and size, in addition to a ten fold increase in MTBF, is anticipated. Concept definition studies are being conducted on the application of on-going VHSIC and related efforts. These programs include the CSP, the EMSP, ICNIA, INEWS, other existing brassboards, and advanced avionics systems that use distributed architecture, common module hardware, integrated racks, data bus and Ada software. The concept definition studies will be continued into 1987.

III.3   AIR FORCE

1. AN/ALQ-131: ELECTRONIC COUNTERMEASURE POD

The AN/ALQ-131 is an airborne pod-mounted Electronic Counter Measure (ECM) system capable of acting against threat radars. VHSIC is being inserted into the AN/ALQ-131 Electronic Warfare (EW) pod through development and retrofit of VHSIC Transmit Control Assemblies (VTCAs). The major goals are to

improve the system MTBF by 25%, reduce the mean time to repair (MTTR) by 50%, provide up to 50% growth space for future capabilities by reducing the printed wiring assembly board count from the existing 16 to 8, provide a common VTCA for all RF bands, and provide an extensive maintenance and diagnostics system (MADS) capability for each VTCA. The MADS system may have wide applicability to future systems. Five VHSIC chips per VTCA (15 per pod) will be required.

Development of the VTCA by TRW began in September 1983, and prototype specifications were delivered in March 1984. The demonstration of the VTCA in the AN/ALQ-131 in December 1985 was the first insertion of VHSIC in an operational system.

Accomplishments for 1986 include the delivery, flight testing, and laboratory testing of the Block I prototype. Initial flight test of the pod occurred on 17 July 1986 on an A-10 aircraft at Eglin AFB in Florida. Work has begun on the breadboard design for the Block II upgrade. If a production decision is made, the Block II VTCA will enter preproduction in 1987.

2. AUTONOMOUS GUIDED WEAPON

The Autonomous Guided Weapon is a standoff weapon which employs an infrared seeker for high value target acquisition (IRHVTA) and tracking. It uses techniques which provide an autonomous acquisition tracking capability, thus eliminating the need for designation and data link information throughout the flight of the missile. The VHSIC technology needed includes the 1750A General Purpose Computer (GPC) and the Multimode Fire and Forget signal and array processor.

A design study began at Texas Instruments in September 1983 and ended in April 1984. The brassboard development was contracted with T.I. in September 1984, and the IRHVTA high speed test effort began in January 1985.

Work has continued in 1986 on the brassboard fabrication and demonstration effort, and on the IRHVTA high-speed test effort. A decision on full scale engineering development will be made in late 1986. The VHSIC processor will be demonstrated in late 1986. Flight tests are scheduled for April through July 1987.

3. COMMON SIGNAL PROCESSOR

A contract with IBM was started in November 1984 for the development of a modular common signal processor (CSP) based on VHSIC technology. It can be configured and programmed to satisfy a wide variety of applications such as high performance radars, secure communications, and electronic warfare. The program is meant to demonstrate the feasibility of a common signal processor using VHSIC, and, in addition, to furnish insights and test results on issues of functional partitioning, module definition, standardization, and packaging software development. VHSIC technology requirements include a 1750A computer, static RAMs, and a number of custom chips designed from the IBM standard cell library.

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Eleven 1.0 micron chips have been designed and will be started through the fabrication process before the end of 1986. A logistics support analysis was completed in September 1986. A demonstration/validation effort for the CSP began in mid 1986. Brassboard delivery is scheduled for December 1987.

4. MIL-STD-1750A COMPUTER

This program will result in processor modules implementing MIL-STD-1750A instruction set architecture for embedded or stand alone applications with VHSIC technology. The computer is designed to operate at 3 million instructions per second and is based on the Pave Pillar common module concept. The VHSIC technology required includes static RAMs and VHSIC gate arrays. There are a total of 21 new chip designs proposed.

TRW/Delco and Westinghouse have been awarded parallel contracts for this work.

Delivery of 11 breadboard modules will begin in March 1987, with two modules being delivered per month. Delivery of 20 Advanced Development modules will begin in March 1988, also with two modules delivered per month. The final software tool set will be delivered in March 1988.

5. PAVE SPRINTER

PAVE SPRINTER is a modular avionics demonstration program. A modular Integrated Communications, Navigation, and Identification Avionics (ICNIA) terminal will be fabricated and tested on the F-111 or F-16 aircraft. It is intended that the VHSIC modular avionics will provide high reliability and two-level maintenance.

Contracts were awarded in October 1983 to TRW and T.I. Fourteen chips needed to meet the modular needs of the terminal were designed by TRW and T.I. The ICNIA design reviews were held in August 1984. A continuation contract was awarded to TRW.

The development of an Integrated Maintenance Information System began in January 1986 and system integration began in April 1986.

The ICNIA brassboard and a 1750A brassboard will both be demonstrated during 1987.

6. AN/ALR-74 RADAR WARNING RECEIVER

The AN/ALR-74 program applies VHSIC technology to a generic modular radar warning receiver (RWR) family. VHSIC technology can provide improved performance as well as reductions in life cycle costs. A study initiated at TRW in September 1984 has been completed. It showed that the preprocessor function can be designed around the Window Addressable Memory (WAM) and Content Address-

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able Memory (CAM) and a VHSIC 1750A chip. No follow on action has been taken.

7. AN/ALR-56C RADAR WARNING RECEIVER

The AN/ALR-56C is the RWR for the F-15 C/D. The RWR is used to detect ground-based and airborne threat radar emissions. VHSIC technology should result in several performance and logistic improvements. The program is expected to make use of several existing VHSIC devices with development required only for gate arrays.

A basic first study by Loral was completed in prior years. A follow on study was scheduled for completion in 1986. An advanced development model development/test is scheduled to begin in 1987.

8. MILSTAR TERMINAL/MODEM PROCESSOR

MILSTAR is an EHF satellite communication system. The use of VHSIC technology will provide improved performance with reduced life cycle cost. It will become possible to install the MILSTAR terminal on platforms with space and weight restrictions that otherwise prohibit such installation. To implement the baseband processor function TRW will use the preprocessor portions of the EHF onboard brassboard as well as the Phase 1 convolutional decoder chip, fast fourier transform chip, and multiplier/accumulator chip.

The program started at TRW in 1984. Detailed hardware design was completed early in 1986. The algorithms and analysis were completed in March, and the first brassboard was scheduled for delivery in November 1986.

The detailed software design will be completed by February 1987. Brassboard fabrication will be completed by March. Hardware and software integration will be performed in May 1987 for a demonstration of the brassboard in July 1987.

9. AUTOMATIC TEST EQUIPMENT (ATE)

Automatic Test Equipment (ATE) is used for operational and maintenance testing of avionics, electronic, and electro-mechanical components on weapon systems and support equipment. The scope of this study is to determine the feasibility of VHSIC insertion in "off-line" ATE with the ultimate goal of developing "suitcase testers". Development of hardware is not within the scope of this study. Contracts started in May 1985 with Honeywell and Sperry. The contracts ended in the first quarter of 1986. Decisions on whether to undertake further work will be made after the contractors' final reports are evaluated.

10. SPEECH ENHANCEMENT UNIT

The Speech Enhancement Unit (SEU) is an advanced development speech processor that removes tone, impulse, and wideband noise from speech channels.

The SEU greatly improves the intelligibility of voice communications for both human operators and speech recognition equipment. VHSIC technology is critical to the implementation of SEUs of a practical size and at an affordable price. The increased throughput and speed of VHSIC will also provide better performance.

The design of a brassboard was begun in 1985 by Westinghouse and Queens College. Fabrication will begin when the design is completed and approved. The brassboard is scheduled to be completed, tested and evaluated by March 1988. Design of the field model will follow.

11. VHSIC PROGRAMMABLE SIGNAL PROCESSOR (VPSP)

The AN/APG-68 is an airborne fire control radar which provides air-to-air target detection and tracking on the F-16 aircraft. A VHSIC PSP would greatly improve the operational characteristics of the radar such as tracking range, target discrimination, and multiple target tracking. The VHSIC technology being designed into the VPSP includes 64K static RAMs and 21 personalizations of a Westinghouse 10K gate array. A 1750A VHSIC chip set will also be required.

A contract was awarded to Westinghouse in September 1985. Some of the VHSIC chips will be supplied by National Semiconductor. During 1986 at least six different gate array personalizations were fabricated. A decision on whether to proceed with the full set of chip designs is scheduled to be made in April 1987. The brassboard and the hardware descriptions will be completed by December 1987.

12. AUTOMATIC TARGET RECOGNIZER

The Imaging Sensor Autoprocessor (ISA) is an advanced development model Automatic Target Recognizer (ATR) being developed by Honeywell to work with a second-generation forward looking infrared (FLIR) system. The ISA will execute algorithms to automatically classify ground targets (tank from truck), provide multiple target tracking, moving target detection, passive ranging, and bandwidth compression for jam resistant data transmission. Application of VHSIC technology to the ISA will allow for multiple scenario system development and multisensor inputs. The improved capability afforded by VHSIC makes it possible to integrate the second generation FLIR to the ATR system. Honeywell's Phase 1 VHSIC chips will be used.

The ATR algorithm was demonstrated in 1983. The VHSIC ATR preliminary redesign was completed in the first quarter of 1986. The final design and validation have also now been completed. A decision to continue with the development is scheduled to be made in early 1987. All hardware fabrication will be completed in 1987.

13. E-3A SIGNAL PROCESSOR

The E-3A SENTRY is the Air Force Airborne Warning and Control System

(AWACS). This insertion effort is aimed at improving the performance and logistics characteristics of the signal processor used in the surveillance radar functional group on board the SENTRY.

A system insertion study was completed in 1983 by Westinghouse. The design phase was completed in 1985. A contract award for the hardware phase was made in August 1986. VHSIC parts production will begin in 1987.

14. VHSIC TTL GATE ARRAY

Numerous Air Force systems contain older transistor-transistor-logic (TTL) devices which are rapidly becoming unavailable. The result is a generation of front line weapon systems that will soon be unsupportable. A majority of the TTL microcircuits can be replaced by a custom VHSIC TTL gate array. VHSIC gate arrays offer such high densities that replacement of TTL devices with VHSIC devices would result in systems with fewer parts and hence reduced long term support costs.

A Request for Proposal (RFP) was released during 1986 for an array design. Contract award is scheduled for early 1987.

15. F-15 CENTRAL COMPUTER

The F-15 Central Computer controls pilot displays, weapon launch solutions and the aircraft G-load warning system. The VHSIC 1750A will form the basis for this program. No new chip development is expected.

The project was approved by OSD in February 1985. Three management options and alternate acquisition strategies have been identified. Funding levels and the acquisition strategy will be decided in 1987.

16. LOGISTICS RETROFIT ENGINEERING FOR MICROELECTRONICS

The Logistics Retrofit Engineering (LRE) program was initiated by the Air Force to solve the growing problem of replacing special ICs that are out of production. The Computer Aided Design/Engineering (CAD/CAE) systems being designed for VHSIC support through the Integrated Design Automation System (IDAS) provide direct LRE simulation and analysis support. System re-engineering with VHSIC technology will improve logistics support through decreased procurements cost and increased reliability.

A generic LRE environment with non-VHSIC capability has been established and tool integration started. The first contract was awarded to Mentor Graphics in August 1984.

Three design projects for the F-111 have been started in 1986. These are the Digital Signal Transfer Unit, Maintenance Control Unit, and the Stores Management System. A chip design is being conducted by TRW. SM-ALC is using a silicon compiler and a conventional design tool from VTI Systems to develop the chip design.

Impact of Electronics on Warfare

Airborne Radar

F-16 VHSIC Programmable Signal Processor

Board

Assemblies	14
Power	800 Watts
MTBF	879 Hours
Performance	40 MCOPS

(W) VHSIC

Improvements

- **More Maintainable/ Less Parts**
- **Built-In Self Test**
- **$300M Life Cycle Cost Savings**
- **Growth Capability**
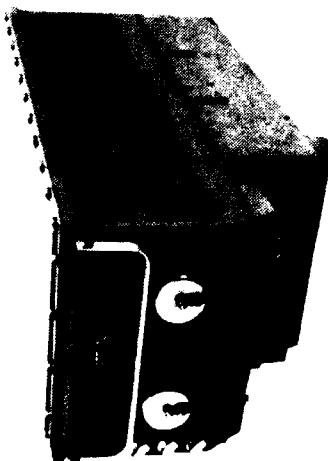
F-16 Programmable Signal Processor
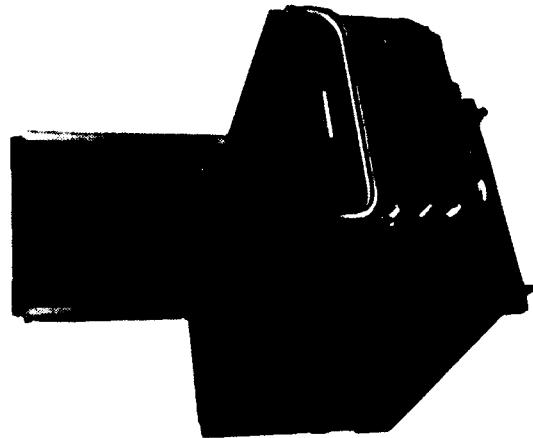
Board

Assemblies	31
Power	2948 Watts
MTBF	275 Hours
Performance	16 MCOPS

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FIGURE III.4

During 1987 the incorporation and verification of IDAS and the VHSIC Hardware Description Language (VHDL) will continue. SM-ALC has also been designated as a Tester Independent Support Software System (TISSS) beta site.

17. GENERIC VHSIC SPACEBORNE COMPUTER (GVSC)

The goal of this program is to develop a high reliability, radiation hardened VHSIC Phase 1 MIL-STD-1750A computer that is qualified for space applications.

The contractors for Phase 1 were selected in July 1985 and included Harris, Honeywell, IBM, and RCA. It is planned to select two of these for the second Phase beginning in January 1987. Since the award of the Phase 1 contracts, a preliminary architecture has been selected and simulated. In addition, test chips have been designed fabricated and tested.

By June 1987 the initial design cycle for Phase two is expected to be complete. The first fabrication cycle and extensive design analysis will then take place between June 1987 and December 1987. Breadboard fabrication will begin in August 1987.

18. ADVANCED ON BOARD SIGNAL PROCESSOR (AOSP)

The AOSP is a general purpose array of signal processing elements which are interconnected through a multiple bus network. The AOSP is a critical system for future space applications such as onboard communications signal processing, radar processing, and electro-optical signal processing. VHSIC technology is required to meet the size, weight, and power constraints of space platforms.

Contracts were awarded in September 1986 for the development of two of the basic building blocks in the AOSP. Brassboards with VHSIC technology will be developed for the Mono Function Signal Processor and the System Input/Output Subsystem. Brassboard demonstration of the AOSP with these two building blocks is scheduled for July 1989.

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SECTION IV

PHASE 2

IV.1 PHASE 0' CONCEPT DEFINITION STUDY

The intent of the concept definition study for Phase 2 was to conduct relatively extensive studies of the submicron technical requirements and system applications prior to undertaking a full scale development program. These studies served as the definition of Phase 2 and an SOW was prepared based on them.

The nine companies that undertook Phase 0' Concept Definition studies were Harris, Honeywell, Hughes, IBM, RCA, Texas Instruments, TRW, Westinghouse, and Western Electric.

As guidance during the Phase 0' studies, the VHSIC Program Office required the IC technology to meet specifications such as:

Feature size	0.5 micron
Functional throughput rate	10^{13} gate-Hz/cm²
On chip clock rate	100 MHz
Failure rate	.006%/1000 hours
Radiation hardening (total dose)	5×10^4 rads(Si)

Each of the Phase 0' contractors was required to investigate the following areas:

o   0.5 micron process development,

o   pilot production of 0.5 micron chips,

o   defect modeling and test structures for yield projection,

o   lithographic and resist techniques for submicron electron beam and optical machines,

o   design tools and design methodology using VHDL in chip design and documentation,

o   support software with Ada as a high order language,

o   testability and fault tolerant design, and specification of a bus interface unit (BIU) for signal interoperability between Phase 2 contractors,

o   system architecture analysis based on projected system requirements.

The nine Phase 0' contractors finished their study programs in January 1984 and submitted proposals in response to the RFP issued for Phase 2. The three

companies selected for Phase 2 awards were Honeywell, IBM, and TRW. Final technical reports for each of the contractors are listed in references IV.1 – IV.9.

IV.2 SUBMICRON TECHNOLOGY DEVELOPMENT

In October 1984, Phase 2 contracts were awarded to Honeywell, IBM, and TRW to continue the technology development for the second VHSIC generation and its demonstration. The technical goals were typified by a minimum feature size of 0.5 micron and a clock speed of 100 MHz resulting in a functional throughput rate of at least 10^{13} gate-Hz/cm^2.

The development activities would be very similar to the activities of Phase 1 except that the goals would be much more difficult and the tools for doing the development would be much less readily available. New tools, new techniques, and more aggressive technical approaches would be needed to achieve the desired goals.

The specific tasks to which the contractors are committed in Phase 2 and the technical requirements of the technology they are to develop are listed in the contractual Statement of Work which is reproduced in Appendix V. There are 8 major task areas:

    (1)   chip technology and fabrication,
    (2)   system architecture design,
    (3)   chip design,
    (4)   support software,
    (5)   interoperability,(BIU) design,
    (6)   module design, fabrication, and demonstration,
    (7)   brassboard design and fabrication (option),
    (8)   design and simulation methodology.

A summary of the approaches proposed by the three Phase 2 contractors is shown in Figure IV.1. The progress and current status of each is separately described below. More detailed information can be obtained from the interim technical reports on Phase 2 which are listed in references IV.10 – IV.14.

Honeywell

The design proposed by Honeywell for an advanced EOSP module required the development of three new chips: a bus interface unit (BIU), a configurable gate array (CGA), and a 32 bit configurable data path (CDP) chip. The specifications of the BIU are being coordinated with the other two Phase 2 contractors in order to maintain interoperability between the three chip sets. For chip fabrication, Honeywell proposed to develop a 0.5 micron bipolar pilot line and to design the transistors for bipolar current mode logic (CML) operation. The process is an evolution of the 1.25 micron bipolar process developed under Phase 1. Honeywell has teamed with Motorola as a major subcontractor for bipolar process development and second source services.

VHSIC PHASE 2 SUBMICRON
TECHNICAL SUMMARY

CONTRACTOR	TECHNOLOGY	DESIGN APPROACH	BRASSBOARD MODULE APPLICABILITY
HONEYWELL	CML BIPOLAR E-BEAM LITHO SINGLE & MULTI-CHIP PACKAGE RADIATION HARD TO 200K RADS	CELL LIBRARY CONFIGURABLE GATE ARRAY 100% TESTABILITY ~80K EQUIV. GATES	RADAR, EO SYSTEMS
IBM	CMOS BULK E-BEAM/U-V LITHOGRAPHY SINGLE & MULTI-CHIP RADIATION HARD TO 200K RADS	CELL LIBRARY MASTER IMAGE CHIP STRUCTURE ~75K EQUIV. GATES	SONAR, EW, RADAR SYSTEMS
TRW	3-D BIPOLAR/CMOS E-BEAM FOR 3-D E-BEAM/OPTICAL LITHO FOR CMOS 1400 MIL SUPER CHIP RADIATION HARD TO 200K RADS	CELL LIBRARY WAFER SCALE INTEGRATION VIA REDUNDANCY ~4M EQUIV. GATES	CRUISE MISSILE, SATCOM, AVIONICS SYSTEMS

FIGURE IV.1

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The submicron processing features electron beam lithography using the JEOL machine, groove isolation, four layers of metal interconnects, and multi-chip packages using thin film, multilayer copper conductors with polyimide dielectrics.

A 7000 sq. ft. Class 10 clean room expansion was built and completed in the Solid State Electronics Division, in Plymouth, MN. This facility houses a JEOL electron beam lithography machines in addition to the advanced fabrication equipment.

During 1986, several changes were made in the module design based on detailed analyses of several different architectures for electro-optical automatic target recognition. The ADAS system level analysis tool was used to do these evaluations. A number of alternative architectural approaches for the brassboard demonstration module have been identified which correct a local bus speed problem. It was determined that operation of the local bus within the module at 50 MHz was not achievable on a board-level, multidrop bus without excessive power penalties. In the new approach, the Image Array Processing Unit and Array Processor Input/Output chips have been repartitioned into one Array Processing Unit (APU) chip), one RAM chip and a new ROM chip. After more analysis and several design modifications, the design goal of an on-chip, register-to-register transfer rate of 50 MHz was reached. It now appears that all the logic chips in this new approach can be designed to fit on the Configurable Gate Array (CGA) chip. This will eliminate the need for the design and fabrication of a large semi-custom configurable data path chip in the core program and thereby considerably reduce the schedule and cost risk associated with the original plan. Optimization of these new chip designs is continuing. The E-O processor analysis and definition task is now completed.

The selection of software primitives that will be coded for the brassboard module demonstration is in progress. The Mentor-SIM translator for cross checking the functional and structural designs is ready for evaluation. The design of software for the microcode compiler was completed and the documentation distributed for review. The detailed design for combining the Verdix Ada front end with the synthesizer of the microcode compiler is now available.

Significantly improved Schottky diode characteristics were obtained by process modifications to eliminate damaged and/or contaminated surfaces caused by dry etching of the surface oxide.

Very good results were obtained with the JEOL E-beam lithography machine in the last half of 1986. The machine was on-line more than 85% of the time. A second JEOL machine has been delivered and installed and is now being used in production. Earlier difficulties observed with beam current fluctuations have been corrected. A proximity correction technique called GHOST, which was developed by Hewlett-Packard, has been used with good results to write first metal layers. A more complete set of proximity corrections for the JEOL is being developed on a subcontract by Harris. A second JEOL E-beam machine has been delivered and is now being used in production. Motorola obtained very encouraging results with their I-line advanced optical photolithography system. Their improved groove process is now very similar to Honeywell's.

Total dose radiation testing of circuit components indicated that this techno-

logy is capable of meeting the total dose requirements for the baseline process, but improvements will have to be made to reach the requirements of the enhanced hardness levels.

Evaluation of lateral pnp transistors for use as load devices in RAM cells indicated that the device will have reproducible characteristics that will meet the circuit design requirements. This is encouraging because this device is smaller in size and has greater potential for SEU hardness than resistive loaded cells. Also, it was determined that higher epitaxial doping was desirable to minimize parasitic pnp effects. Early results with an optimized graded epitaxial process were very favorable.

Thermal aging tests on solder bumps used in single chip package assembly completed 1000 hour tests successfully. Although the solder appeared very stable, a nickel layer could be used as a barrier to stop diffusion of tin. A new solder process, with more controlled solder reflow, was used with the tape automated bonding lead frames obtained from 3M. Good solder bonds to lead frames were obtained, having average bond strengths of greater than 20 grams in pull testing.

A spray coating process for the deposition of polyimide on multichip package (MCP) substrates was fully characterized and included in the baseline process. Spray coating improves throughput and reduces edge bead formation. The baseline MCP fabrication process was demonstrated successfully by the fabrication of ring oscillator and thermal test vehicles. Test data indicated that the package will support 100 MHz designs. Fabrication of MCPs with pinned substrates began. Early test results indicated that good uniformity can be achieved with sputtered metal layers. A technique for removing an individual die from a MCP was demonstrated. The design and layout of a nine-chip MCP for the circuit technology test chip (CTTC) were completed. This 3.25x3.25 inch package will be the first MCP to be fabricated and tested.

Multilayer metal yield test vehicles were completed through five metal layers, with continuous via chains through all five layers. However, some via resistance are presently too high. Ring oscillator tests at 25 microns and 40 microns dielectric thickness (for different characteristic line impedances) are in progress.

A third JEOL E-beam lithography machine will be brought on line during 1987. Process control techniques to reduce defect densities and rework will be developed. Intermixed optical/E-beam lithography will be used to increase wafer throughput and decrease process time. A fully planarized, four-layer metal process will be verified. Yield and performance models will be developed to predict the yields of 0.5 micron VHSIC chips.

Design automation tasks will include the evaluation of VHDL tools, completion of the VHDL-to-Mentor translator, continued work on the structural design verification tools required for the BIU chip, completion of placement and routing of the BIU and various test cases, and floorplanning of the APU and APC chips.

In the area of second source development, Motorola received the Perkin Elmer AEBLE-150 E-beam lithography machine in October 1986 and is bringing it into operation. They will continue to evaluate the feasibility of using submicron optical photolithography with an I-line lens.

During 1985, IBM successfully transferred the 1.0 micron CMOS process capability to the Federal Systems Division in Manassas, VA from the General Technology Division in Burlington, VT. Joint efforts with the IBM Research Division in Yorktown Heights, NY were active during this same period to establish E-beam 0.5 micron lithography capability at the Manassas site. The 0.5 micron E-beam facility construction was completed ahead of schedule in October 1985, and tool installation began. This facility is a critical component for the program.

Extensive simulations of device designs, process models, and ground rules were performed and the first version of the IBM 0.5 micron CMOS process ground rules was released to logic designers. The first attempt at fabricating chips began with two sets of nine test wafers which included 1.0 micron horizontal and 0.5 micron vertical feature sizes. Parametric data proved to be excellent. Engineering analysis related to the technical challenges posed by enhanced radiation specification was well underway by mid-1985. Experiments were in process to attack the areas of total dose, single event upset, and latchup susceptibility.

Design strategies for chip testability were put in place to ensure that the aggressive VHSIC Phase 2 program goals for improved component and system level testability would be met. Ground rules were provided to logic designers.

The master image design approach and computer aided design tools developed during the VHSIC Phase 1 program were improved and extended to support chip designs and testing. The development of the macrocell library, which is critical to the master image design methodology, was almost 90% complete by the end of 1985. Design requirements for all four Phase 2 chips were completed in 1985. The 1.0 micron version of the configurable static RAM (CSR) was released for fabrication in November 1985.

In the packaging area, progress included the establishment of detailed engineering specifications for the single and multichip packages and connector hardware. The first single chip and multichip prototype hardware was received and extensive qualification testing was started. Interim test results from this prototype hardware were extremely encouraging.

A major accomplishment during 1985 was in the area of interoperability standards. Work began on the VHSIC standard PI and TM buses in December 1984, and by June 1985 preliminary detailed specifications were available for review by Government representatives.

Early in 1986, the VHSIC 1.0 micron macrocell library was completed and work was began to automatically convert this library from 1.0 micron to 0.5 micron. The library contains all master image macrocells for the four VHSIC chips being fabricated under the Phase 2 program.

Nine more test wafers were completed in March 1986. These wafers have functional circuits in full 0.5 micron feature sizes. The 1.0 micron systolic

processor (SP), bus interface unit (BIU), and address generator (AG) chip designs were released to fabrication in February, April, and May 1986. The SP chip contains 33,000 gates on a 5.5x5.5 mm chip image. The functional throughput rate (FTR) will exceed the program goal by 10 percent. The chip power is projected to be 0.8 watts.

The 1.0 micron versions of the CSR and the BIU have been fabricated and 100% functionality has been verified under slow speed, room temperature conditions. The fabrication of the AG chip was completed by late December. Completion of the SP fabrication and then functional testing of the AG and SP are scheduled for early 1987.

The development of the brassboard module for the large acoustic array beamformer reached a major milestone with the completion of the multiwire package test board. This test board will host the single chip equivalent of a current multichip package containing 16 chips. In addition, the installation in an IBM PC of the test driver software for the brassboard module was completed ahead of schedule. Full simulation of the 16 chip multichip package containing the four chip types required in the Acoustic Beamformer was completed. The brassboard module test bed is essentially complete. Functional testing will begin after the first versions of 1.0 micron CMOS chips become available.

The E-beam tool has been used during 1986 to process various submicrometer parts. The tool has performed well and has consistently demonstrated stability in the in-line parameters.

Radiation enhanced process development continued during 1986, with excellent test results. IBM parts fabricated with the enhanced process were tested in the University of California cyclotron in November 1986 to gather single event upset data.

Analysis of single chip packages supplied by a vendor was completed in 1986. Improvements were developed based upon this analysis. Improved hardware was ordered and received in May 1986 and is currently under engineering analysis. Testing of prototype multichip hardware continued during 1986. These prototypes have completed 1800 temperature cycles performed in accordance with military specifications with no failures.

A VHDL translator specification was completed and work was begun to code and debug this translator. Activities to complete the Parallel Interface (PI) bus and Test and Maintenance (TM) bus specifications continued during 1986 (see Section IV.3 below).

During 1987, the major Phase 2 program activities will include:

o   continued development of the enhanced radiation hard fabrication process,

o   completion of the design of the 0.5 micron BIU to incorporate multicast suspend,

o   functional and parametric testing of the 1.0 micron version of the Phase 2 chip set,

o fabrication of the 0.5 micron versions of the AG, SP, CSR, BIU chips, and the 1.0 micron CMOS SPE,

o fabrication of all beamformer brassboard module components and completion of tests on the 1.0 micron version of the beamformer module.

TRW/MOTOROLA

The TRW/Motorola approach is based on four principal tasks:

o a superchip design concept which results in chips between 1.0 and 1.4 inches on a side containing from 5 to 20 million transistors (see below),

o process technology development which would result in a 0.5 micron bipolar process at TRW and a 0.5 micron CMOS process at Motorola. The delivery and use of the AEBLE-150 E-beam lithography system, which was developed in Phase 1 by Perkin Elmer, was critical to this task. Motorola expected to have the AEBLE-150 by November 1985 and TRW by December 1985.

o packaging for superchips, modules, and brassboard,

o systems engineering and application, including hardware and software, for the module, the brassboard, and the total system.

The superchips proposed by TRW are based on the concept of using massive redundancy at a cellular level in order to achieve very large scale functionality in a chip which can be produced at very respectable yields (10% to 50%). The resulting chip is huge by any standard - up to 1.4 X 1.4 inches. The redundant structures in the chip are all available for testing by an on-chip test node, and if they are functional they are switched into operation. If they are not functional, the test node proceeds to test the next redundant structure. All this testing and switching is done automatically on "power up" and is referred to as reconfiguration of the chip. In order to ensure adequate yield and reliability of the interconnections between the test node and the redundant cells, the information busses are made triply redundant.

In 1982, TRW had started an internal IR&D program to design a very large memory (VLM) chip to validate the superchip concept and obtain the data needed to proceed to larger and more complex superchips. This work has been used as the basis for the Phase 2 design approach. The other principal vehicles needed for verification are two proof of concept (POC) chips.

The VLM is a 750K static RAM fabricated in CMOS, using 1.25 micron optical lithography. The POC chips are portions of the superchip CMOS mass memory chip and the bipolar convolver chip, each containing more than 4000 gates and chosen to include representative macrocells. The POC chips would be fabricated with the baseline bipolar and CMOS processes at 0.5 micron.

Processing: For the 0.5 micron bipolar technology, TRW has been modifying the Phase 1 triple diffused process to include a self-aligned polyemitter process, trench isolation, ion implanted arsenic resistors for improved resistance and temperature characteristics, and triple level metal. The process requires a total of 13 mask levels, all of which would be defined by E-beam lithography.

During 1985, TRW experienced inconsistent results with the polyemitter process when it was transferred from optical processing to E-beam processing. There were also difficulties with some of the interlayer dielectric materials. Poor device parameters on test chips were traced to high contact resistance at the emitter and at the collector ring. Other problems with the three level metalization system appeared. The lack of the AEBLE-150 E-beam machine during this time slowed down the gathering of experimental data needed to diagnose and correct the problems. The Cambridge EBMF-2 electron beam machine which has been used for processing, has a very slow exposure time. This resulted in very long test chip processing time and, consequently, very slow gathering of data upon which further experiments could be based.

Motorola, meanwhile, was developing the submicron CMOS process based initially on using p-/p epitaxial wafers, trench isolation, 150A gate oxide, polysilicon gate, sidewall oxide for source and drain definition, partial planarization for first metal, and oxide planarization for second metal. During 1985, the effort focussed on development of the trench isolation process and improvements in metal deposition. Delivery of the first AEBLE machine to Motorola was initially projected for August 1985, but delivery was delayed until October 4, 1986.

By the end of 1985, the slip in the AEBLE-150 delivery schedule was adversely affecting the program goals and milestones of both Motorola and TRW.

Starting in 1986, TRW began to transfer the submicron bipolar processing to a new facility. Emphasis was placed on solving the polyemitter processing problem and the various other metalization difficulties. It became apparent that the causes of the problems had not been sufficiently identified and corrected to establish the baseline process needed to fabricate chips. The continued slip in AEBLE-150 delivery minimized the possibility of recovering the lost time. A decision was made to discontinue the bipolar process development and make all chips in CMOS using the submicron CMOS baseline process as defined by Motorola in March 1986.

The AEBLE #1 system has undergone factory performance tests and Motorola accepted the machine on July 31, 1986 with a number of exceptions on performance which Perkin Elmer is to correct. Phase 2 processing of test wafers is continuing at Perkin Elmer on the prototype machine until the Motorola machine is in operation in Phoenix which is expected to be in January 1987.

Design: Preliminary tasks concerning design management, hierarchy, methodology and testability were started in November 1984. This early work also emphasized BIU chip specifications and interoperability considerations. Effort on the convolver and signal processing superchip requirements and specifications began in March 1985, as did the architectural and design considerations of 3D and CMOS macrocells. At this time, a broad base of design tools was being imple-

mented. The baseline design methodology for all chips was to do a top down decomposition of the chips. The sparing concept which underpins the superchip concept begins at the macrocell level and continues through the function level. During 1985, the design requirements and detailed circuit structures of the superchips, the POC chips, the large macrocells, and the BIU chips were begun.

By June of 1985, preliminary design of the 3D POC chips and many of the macrocells for the superchips were initiated. The POC chip would verify the macrocell design, testing strategy, and the reconfiguration methodology. The BIU definition started in July/August 1985. The BIU architecture included a parallel interface bus (PI), a test and maintenance bus (TM), and a chip to chip bus (CC). TRW began plans for application of VHDL in Phase 2. Superchip timing analysis requirements were established by September 1985, with plans to use a Daisy timing verifier integrated with a VAX computer. Preliminary superchip design rules for CMOS and 3D were established with Motorola agreement on CMOS. By the end of 1985, substantial progress had been made in the design and architecture of the superchips, particularly the convolver. BIU definition was nearing completion. Both the CMOS and bipolar POC chips were designed and layout was well underway. The fabrication of the VLM chip was projected for mid-1986 and actually accomplished in December 1986.

During 1986, the CMOS component library was completely reworked to accommodate design rule changes. Layout started on the convolver macrocell and POC test chip, and CMOS macrocell design was initiated. The CMOS 4K SRAM POC was completed by 2 May 1986, and processing started on the AEBLE 150 #0 machine. To verify POC logic, a switch level POC with two kernels and I/O circuitry was assembled. The first POC wafers were completed in August. No functional circuits were obtained due to E-beam registration problems.

A VHSIC Design Handbook has been written and became available in September 1986. The POC test chip layout is complete and logic verification is 90% complete. Much of the design activity for the CMOS macrocells for the Systolic Processor Superchip is nearing completion. BIU logic design, simulation, and schematic capture are underway.

Packaging: TRW is developing a "buttonboard" concept for module-to-module electrical interconnections. The buttonboard may be viewed as a circuit board with a dense array of holes, each filled with a dense wad of fine gold plated wire called a "button". This board is sandwiched between two module boards, and pressure on the wire "buttons" serves to make contact. A mechanical mockup of the cruise missile processor brassboard was designed to verify the button board configuration and other characteristics. This interconnect verification test module (IVTM) contained 6000 buttons. By December 1985, the IVTM design was complete, and button boards and hermetic chip packages were on order.

At the beginning of 1986, the chip package candidates being considered were ceramic, as the baseline, and metal. Heat dissipation, attachment of the die, and other packaging details are especially important because of the large physical size of the superchips. In January, the chip attach tooling was 85% complete. Superchip attachment simulation was begun, using large Phase 1 CAM wafers under various degrees of power dissipation. A detailed 320 pin superchip package design was generated, and Bourns indicated immediate capability to deliver. An

alternative metal chip package was designed. Work is continuing to address these problems.

System Engineering: TRW selected the improved cruise missile as the system candidate for superchip brassboard module applications. The specific module to be built will demonstrate advanced EW processing for target recognition and acquisition and self protection. Preliminary chip specifications to achieve the brassboard functions were completed, and a submicron superchip set defined to implement a module and a full brassboard. A full cruise missile brassboard would also include a CMOS associative processor, a CMOS fast Fourier transform chip, and a CMOS data processor. The TRW/Motorola 0.5 micron superchip set for the module includes a convolver superchip (bipolar), a mass memory superchip (CMOS), a signal processor superchip (CMOS), and a bus interface unit (CMOS). The Phase 2 brassboard module for system demonstration is based on EW and RADAR algorithms. The module specifications for the three superchips, the BIU, and the system support software have been completed.

Functional specifications were prepared in early 1986 for both the SPS and the CS. The MMS will be delayed until late 1986 since it requires the SPS design as a precursor. Interoperability resolution has delayed the BIU requirements specification until December 1986. Architectural simulation of the EW system application was initiated in January 1986. A major problem developed with the CS design in terms of yield, chip area, and power dissipation because of the difficulties with the bipolar processing development. In September 1986, TRW proposed to the Navy that the CS chip be fabricated in CMOS. The proposal is currently under consideration. The macrocell architecture definition of the SPS is essentially complete. A revised BIU requirement specification was produced.

IV.3   INTEROPERABILITY

One of the tasks of the Phase 2 contracts is the requirement to establish interface/interoperability standards to assure that all chips developed under Phase 2 can work together electrically and physically (paragraph 3.5.1 of the Phase 2 Statement of Work, Appendix IV). The standards are to be established by agreement among all VHSIC Phase 2 contractors and the VHSIC Program Office.

To carry out this task, the VHSIC Program Office established a tri-Service Interoperability Committee with representatives from each of the three Services and each of the three Phase 2 contractors. The accomplishments that have been made under the program so far are discussed below.

An electrical interface specification has been developed and released by the contractors (Version 1.3, 20 March 1986). See reference IV.15. In particular, it defines the standard VHSIC chip I/O voltage levels and drive currents. In addition, it defines the standard VHSIC chip power supplies as +3.3V +/-5% and +5V +/-10%.

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A standard system interface bus has been developed. It has been named the PI-Bus (Parallel Interface Bus) and will connect up to 32 modules on a backplane. Depending on the loading, it can run from 12.5 MHz (full load) up to 25 MHz (lightly loaded). The bus provides a choice of 16- or 32-bit wide data paths, in either an "error detection" or a "single error correct, double error detect (SECDED)" mode. These modes may all exist simultaneously on the same backplane. In the past year, in order to meet 1750A/CSP requirements and to satisfy changes requested by an industrial standards group (SAE AE-9B), a multi-cast suspend mode has been incorporated into the bus operating protocol.

Version 2.1 of the PI-Bus specification has been released. Each of the three VHSIC Phase 2 contractors is building a BIU to operate to this specification. The PI-Bus specification exists as a copyrighted document, and may only be copied in its entirety. The purpose of the copyright is to prevent the reproduction of multiple unauthorized versions of the PI-Bus. Users must quote the document in full, and state any exceptions which exist in their implementation. See reference IV.16.

A second standard system bus has been defined called the Test and Maintenance Bus (TM-Bus). It is a serial backplane bus. Version 1.2, dated 31 August 1986, includes improved definitions of message protocols, broadcast capability, multicast capability, and TM-Bus interrupts. It now references the electrical specification of the PI-Bus for consistency since these two busses will be used concurrently on a backplane. The TM-Bus supports a full range of clock frequencies from 0 Hz to 6.25 MHz. See reference IV.17.

A second maintenance bus, the Element Test and Maintenance Bus (ETM-Bus), has been specified to provide a well defined test port for all VHSIC chips. Its purpose is to provide an interface by which any user may connect to a VHSIC chip's maintenance port in a standard manner. The actual test instructions issued to the chip are a function of the class of built-in-test provided by the chip manufacturer and are not provided by the specification. It does provide for ring, star, or tree configurations (depending on system requirements). Version 1.1 of the ETM-bus, dated 31 August 1986, references the electrical specification section of the PI-bus for consistency. See reference IV.18.

The contractors are also working on a standard clock specification and the definition of a point-to-point bus for system data flow.

With the completion of the above two items, it has been agreed by the Interoperability Committee that both the letter and the spirit of the SOW requirement will have been achieved. It is projected that the definition of the standards will be essentially complete by January 1987. Following that, it will only be necessary to maintain the specifications (including minor corrections and elaborations) and to ensure that the contractors comply with them.

SECTION V

PHASE 3 - SUPPORT TECHNOLOGIES

VHSIC Phase 3 is a support technology program which began in 1980. In contrast to Phases 1 and 2, which are large, comprehensive, multi-technology programs, Phase 3 consists of shorter projects with limited objectives in the areas of key technologies, equipment, and tools. It has run concurrently with Phases 0 and 1 and is continuing during the Phase 2 period. Projects completed prior to 1986 are discussed in Section V.5.

V.1   INTEGRATED DESIGN AUTOMATION SYSTEM (IDAS)

The design automation portion of VHSIC technology is currently being developed under the Integrated Design Automation System (IDAS) program. Design automation work under VHSIC actually predates the IDAS program. Work had begun during VHSIC Phase 3 in 1980 with the investigation of some design tools. The most notable of these were the Architectural Design and Analysis System by the Research Triangle Institute and a study of hardware description language requirements by Sperry.

The formal IDAS program began in late 1980 with plans for developing a VHSIC hardware description language (VHDL) and other tools for the efficient design, documentation, and management of VHSIC hardware and software. In order for the tools to be useful in the insertion of VHSIC technology into systems they must be able to reduce design time and cost significantly. In particular, it is desirable to develop tools which automate the initial stages of the design process at the system level and make it possible to assess the effects of various hardware/software tradeoffs very early in the design process. The designs can then be more responsive to system requirements. The tools must each not only be capable individually of handling designs of VHSIC complexity but they must also be integrated into a smoothly working ensemble. This latter goal is achieved by requiring that all tools be capable of accepting designs expressed in the VHDL. In addition, if a tool operates at the algorithmic level, then, where feasible, the algorithms should be expressible in Ada as a common high order language.

Finally, the tools produced under this program must be of sufficient practical utility in the design process that they will find ready acceptance in the DoD community. The use of these tools is being especially promoted at Service in-house design centers.

The IDAS program is organized into the four major task areas described below. The contractors active in the development of IDAS are listed in Appendix II.

1. VHSIC Hardware Description Language (VHDL)

The DoD faces the need to procure and maintain systems over a twenty year life cycle. The design tools that are created under VHSIC must automatically produce full design documentation as a natural part of the design process. The VHDL program was initiated in order to establish an industrial standard for the documentation of the VHSIC process and products. The work is composed of the following elements:

- o VHDL language definition and development,
- o VHDL Independent Validation & Verification (IV&V),
- o Air Force Institute of Technology (AFIT) support,
- o Joint US/Canadian IBM Rehost.

The definition and development of VHDL is the cornerstone of the IDAS program. A schematic description of VHDL is shown in Figure V.1. A one year program definition phase was started in July 1983, with a team consisting of Intermetrics (prime), IBM, and Texas Instruments. Implementation of software started in August 1984 and will continue until March 1987. Two partial releases of software have been made to date - one in January 1986 and one in July 1986. The software being developed includes an Analyzer, Design Library Manager (DLM), Reverse Analyzer, Simplifier, and Simulator. The final release is due in March 1987.

The purpose of the IV&V effort is to test the VHDL software in actual use in the field. The primary contract for this effort was awarded to the United Technologies Microelectronics Center (UTMC) in August 1985. The work is divided into two parts. The contractor performs an initial test of the VHDL software and then acts as a focal point for secondary testing at "beta" sites. During 1986, UTMC has evaluated the two partial releases of VHDL software and has distributed them to beta sites snown in Figure V.2.

The AFIT is serving as one of the beta sites as well as providing other support functions for the VHSIC program in relation to the VHDL. It is developing UNIX-based VHDL tools to distribute to universities, teaching VHDL in its CAD curriculum, providing consulting support on the IEEE standardization effort, and developing short courses on the VHDL for Government personnel.

The standardization activity which AFIT supports started in 1984 with discussions between the DoD and the IEEE Design Automation Standards Subcommittee (DASS) and the Standards Coordinating Committee 20 (SCC20) of the ATLAS group. A formal VHSIC standardization committee called VHDL Analysis and Standardization Group (VASG) was formed. VASG was chartered in March 1986 under the DASS. VASG is addressing the issues which arise in the standardization discussions and is developing a revised language reference manual. Final approval of the standard VHDL is expected by March 1987 and is currently on schedule.

Under the Joint US/Canadian VHDL IBM Rehost program, the VHDL tools are being adapted for use with IBM mainframes. The US will provide the VHDL software and technical consultation. The Canadian contractor, Bell Northern
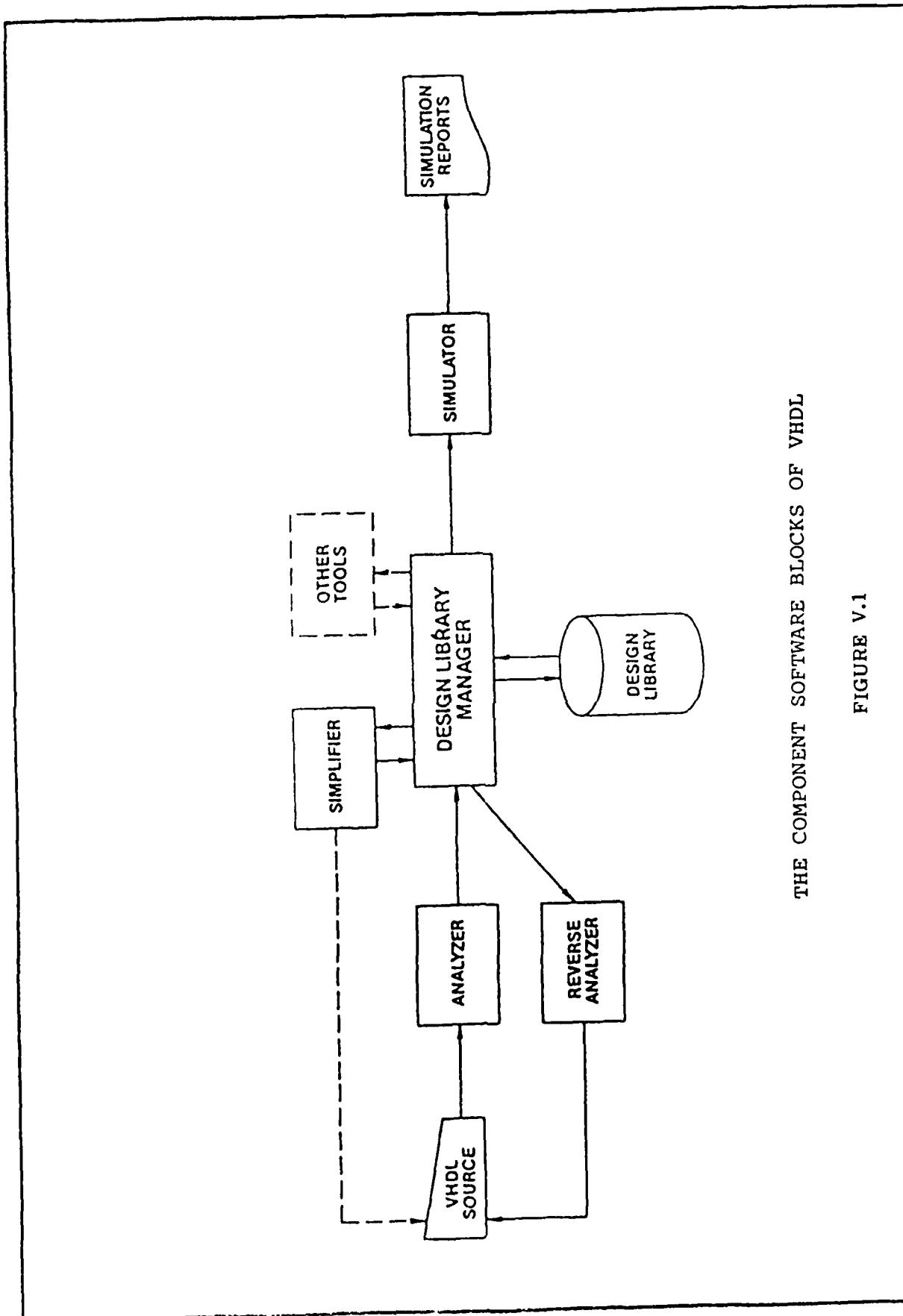
THE COMPONENT SOFTWARE BLOCKS OF VHDL

FIGURE V.1

VHDL IV&V

16 GOVERNMENT FUNDED BETA SITES

6 DOD/CONTRACTOR SITES

ARMY
NAVY
AIR FORCE

HONEYWELL
TRW
IBM

10 UNIVERSITY SITES

ARIZONA STATE
AUBURN UNIVERSITY
CARNEGIE-MELON
CASE WESTERN RESERVE
GEORGIA INST. of TECH
U of MONTREAL
VIRGINIA TECH
U of WATERLOO
RPI
USC

FIGURE V.2

Research, will install the VHDL software in the IBM machines and integrate some of its own design tools into that VHDL environment.

2. VHDL Technology Insertion

The VHDL Technology Insertion program provides advanced design tools to support the designer using the VHDL. Beginning in August 1985, nine contracts have been awarded as listed in Appendix II.

a) Workstations/Interfaces (GE, Gould, APL)

The purpose of these efforts is to develop terminals and interfaces which assist the designer using VHDL. General Electric is developing a workstation suitable for production use. The first of five prototype workbenches using a Symbolics terminal was completed in November 1985. A complete chip design will be used to demonstrate the workstation environment. Gould is designing a generic workstation interface for VHDL, using a SUN 3 workstation, which will automate the generation of VHDL code and check for internal consistency. One workstation was installed at the Ft. Monmouth ETDL in 1986. The Johns Hopkins Applied Physics Lab (APL) is writing software translations between the VHDL and existing languages such as ADLIB/SABLE and ISP', and is integrating the tools around the VHDL internal form IVAN.

The APL effort has proceeded on schedule and will be completed by the end of 1986. Translators have been easily and quickly developed between the Mentor Graphics workstation and VHDL and between VHDL and ADAS. For example, the translation of a limited set of constructs needed for their work was completed in a matter of a few weeks. This has been done using the OPS-5 expert system program which runs on the VAX.

b) Analysis Tools (RTI)

The Architecture Design and Analysis System (ADAS) is a set of directed graph tools that were initially developed under VHSIC funding during VHSIC Phase 3. The tools are useful for modeling algorithms and architectures and then assessing their performance. RTI is now interfacing the ADAS tool set with the VHDL. A 24 month contract was awarded to RTI in 1986 to enhance ADAS and to integrate ADAS with VHDL and its support environment. ADAS has already become a widely used tool within the VHSIC community. The RTI system is being installed at 20 Government sites.

c) Synthesis Tools (Honeywell, JRS Research, Sperry)

The purpose of these efforts is to derive chip design data automatically from a VHDL behavioral description as illustrated in Figure V.3. The Synthesis Tool effort by Honeywell was the MIMOLA software system to determine a useful chip architecture from input that is algorithmic in nature and contains an implied structure. The product is an architectural description of a microprogrammed device in VHDL and the microcode to drive the device.

Application Specific Architecture

Synthesis
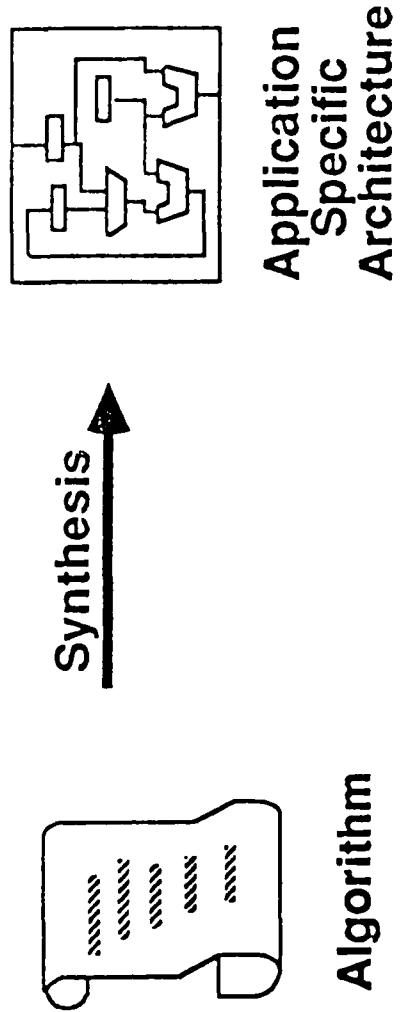
Algorithm

Behavioral Synthesis:
From Algorithm to Architecture

FIGURE V.3

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JRS Research is developing an Automated VHDL/Microcode Compiler Synthesis and Design System (AMSDS) which synthesizes a microprogrammed processor architecture from an Ada program and a VHDL description of chips. Output from the program is a VHDL description of the processor and an optimized microcode for the processor. The microcode compiler portion of the system is automatically retargetable from an external VHDL processor description.

Sperry Corporation is developing software to simulate the performance of hardware described in VHDL. The proposed Sperry simulator provides simulation with mixtures of functional and structural specifications.

An interactive simulator using a different hardware description language has already been developed in-house by Sperry. Sperry has undertaken to determine whether its MIXSIM Simulator can be modified to fit into the VHDL. The company has concluded, based on this study, that the project is feasible and is proceeding with the actual development of the simulator.

Most of the coding for AMSDS was completed during 1986 and will be tested in 1987. The ability to drive the compiler from VHDL machine descriptions and the ability of the microcode compiler to accept Ada source code are both important steps in breaking the bottleneck of laboriously hand coding microcode. Microcode is the heart of many VHSIC chip designs. Being able to quickly perform trade-offs between algorithms, hardware and microcode implementations (using the VHDL simulator) will also be extremely valuable in speeding up and optimizing the design process.

d) Silicon Compiler Interfaces (RTI, National Semiconductor)

RTI is developing an interface between the VHDL and the Gensil compiler of Silicon Compiler, Inc. As the chip is compiled by Gensil, a VHDL description is automatically written. The CMOS interface effort by National complements this by producing the chip designed with the Gensil compiler on the National Semiconductor CMOS VHSIC pilot line. This provides an experimental demonstration that the hardware output corresponds to the input design specifications.

3. System Design Tools

This program is developing advanced design tools aimed at making the higher (system) level of the design process more automated and more efficient. There are currently nine specific contracts in this area that will provide a variety of tools in areas such as design verification, design for test, advanced system synthesis, and life cycle cost modeling. These items are currently in procurement under a Project Research and Development Announcement (PRDA). Some contracts have been awarded starting in September 1986.

a) Annotation Language for VHDL (Stanford)

This tool provides a designer with an English-like language in which to write requirements. These requirements can be inserted into the VHDL design and extracted by a verification tool to insure that a design meets the set of specified requirements.

b) Advanced Ada Synthesis Tool (to be awarded)

This tool will extend the capability of synthesizing system architectures which can handle networks of synchronous machines in an asynchronous system. It will provide the capability to produce a VHDL model of the machine from a VHDL library of either full chip descriptions or minicell descriptions. For automated chip synthesis, an interface to a silicon compiler is provided so that a designer can input an Ada algorithm and get silicon out with a VHDL description. The tool also provides optimized microcodes for the device synthesized.

c) Advanced Component Design Using VHDL (to be awarded)

This effort will provide an interface between the VHDL and the University of Southern California (USC) silicon compilation tools. The input will be a VHDL description and the output will be a verified component tape ready for manufacture. In addition, an advanced requirements language with a limited English vocabulary will be interfaced for formal verification.

d) Hierarchical Design for Testability (RTI)

This effort was started in September 1986 by RTI and will result in a set of knowledge based rules, using artificial intelligence techniques, for the ADAS system. It will help a designer automatically develop testable designs as the design process progresses.

3) Analog Design with VHDL (to be awarded)

This effort will explore the utility of VHDL in analog component design and recommend extensions to the language which may be needed for analog design purposes. A prototype analog design system will also be constructed.

f) Object Oriented Chip Design Using VHDL (to be awarded)

An advanced design tool will be developed that uses a novel way of producing a design. The designer will have available a set of "components" or building blocks in a library from which he can build a chip. These blocks will be keyed like jigsaw puzzle pieces so that the design process will be essentially like putting a jigsaw puzzle together. As the designer puts the design together, the VHDL description and the chip physical layout will be produced automatically.

g) Artificial Intelligence Interface to the ADAS
   System (RTI)

RTI was awarded a contract in September 1986 to develop the capability to map a set of software application programs onto a multiprocessor network with constraints. For example, if the set of programs must execute within a given time, this tool will determine all of the ways that the set of programs can be configured on the set of processors so that the execution time will be less than the constraint.

4. Engineering Information System (EIS)

Any IDAS requires a framework within which hardware and software information can be managed from the inception of a design through its complete life cycle. The EIS will allow data to reside in a heterogenous hardware environment but present a homogenous view of those data to the designer. The DoD is working with industry and the IEEE to obtain a common standard. A joint DoD/IEEE workshop was held at the University of Arizona in January 1986 to generate EIS requirements.

This program is now in the procurement process with the RFP distributed in August 1986. Contract award is expected in 1987.

V.2 LITHOGRAPHY

1. E-Beam Lithography

The development of E-beam lithography equipment with a capacity for high wafer throughput was considered to be necessary for fabrication of 0.5 micron feature size VHSIC chips on a pilot line basis. The system consists of an electron-optical column, work chamber, stage, vacuum system, system software, deflection and pattern exposure circuitry, automated loading system and a pattern data interface which is compatible with the VHDL design language. Wafer processing capacity (throughput) is specified to be at least four, four-inch diameter wafer levels per hour.

A three year contract effort was awarded to Hughes Research Laboratories in May 1981 with Perkin Elmer Corporation as the major subcontractor. See references V.1 – V.3.

The VHSIC E-beam machine is a direct write lithography system capable of writing 0.5 micron patterns typical of those which will be required for the VHSIC Phase 2 chips. The wafer processing capacity of the system is 4 to 25 four-inch wafer levels per hour depending on the writing requirements, pattern density, and resist sensitivity. This throughput level is adequate for moderate production needs.

System support software is an interface between the VHSIC design center and the E-beam exposure mechanism. The support software has been designed so that the VHSIC chip designer needs no knowledge of E-beam Lithography apart from a set of design rules.

The hardware system consists of the following elements:

o   a pattern generator to generate the E-beam deflection data,

o   a mechanically driven stage which positions the wafer under the electron beam,

o   an electron optical column with a high brightness lanthanum hexaboride (LaB_6) electron source optimized for 20 kV operation,

o   a cassette wafer handler which feeds 25 wafers at a time to the system, [Each wafer is individually transported from the input cassette to the wafer aligner, then to a pallet which glides on rollers to the work chamber. When wafer exposure is complete, the pallet is removed from the work chamber and transported back through the lock and airlock chambers to the output cassette.]

o   an operator console which provides the system with a centralized interactive terminal from which system operation is controlled. [The primary operator is provided a display terminal CRT and keyboard.]

During 1986, the first phase of development of the system software support and control was completed. To date, Perkin Elmer has received six firm orders for the AEBLE-150, including orders from three VHSIC contractors – TRW, Motorola, and Hughes. The first machine was delivered to Motorola on October 4 1986.

2.   X-Ray Lithography

The objective of the X-ray program is to develop a lithographic tool which can reduce the cost of producing submicrometer chips for moderate volume technology insertion. An X-ray step-and-repeat lithography machine for this purpose must be capable of 0.5 micron (and less) line width and/or space resolution and have a throughput of at least 20 wafer levels per hour (with a 10 mJ/cm² resist sensitivity) for four inch diameter wafers. An X-ray mask vendor source is also needed for the fabrication of suitable masks. A further increase in the throughput of the X-ray machine by 2 to 3 times is projected from the development of a pulsed plasma X-ray source. This will have 10 times the intensity of the base line source (electron beam impact on a high atomic number metal).

The X-ray stepper machine is scheduled to be installed and tried out in a VHSIC Phase 2 pilot line to determine its patterning and throughput capabilities.

The VHSIC X-ray lithographic prototype machine development program includes the following tasks:

o   development of an X-ray step-and-repeat (XSAR) machine (with electron impact source) by Perkin Elmer, starting in December 1983,

o   development of a high brightness X-ray source by subcontractor Maxwell Industries, starting in January 1985,

o   installation and operation on Phase 2 Pilot line by Perkin-Elmer and subcontractor Motorola, commencing in early 1987.

All three tasks are part of one contract of which Perkin Elmer is the prime contractor.

A contract award was made to Perkin-Elmer in December 1983, for a 33 month contract for the X-ray stepper development. During the first twelve months, the work concentrated upon preliminary specifications review in which the X-ray stepper system error budget allowances were determined. Subsystems (anode and E-gun, aligner, electronics control and data handling, vacuum and mainframe, and masks) were likewise analyzed and assigned detailed error allowances. Mechanical, electronic, and optical hardware items related to subsystem and system designs were reviewed and a system preliminary design was established.

During 1985, the system design was fixed and the error budget allowances were set to achieve 0.3 micron patterning resolution. A water-cooled tungsten anode rotating at 8000 RPM was designed to dissipate 10KW of power into a 1.5 micron spot. Fine lateral alignment of 0.1 micron was achievable with a zone plate-grating detection scheme and a single visible HeNe laser beam source.

In January 1985, a contract modification initiated an eighteen month program with Maxwell Industries to develop pulsed plasma, high-brightness sources. The high-brightness design was partially assembled (modulator, power supplies, control electronics, and data handling console).

Perkin-Elmer initiated the establishment of an X-ray mask fabrication facility at its subsidiary company, Applied Lithography Operations (ALO).

The X-ray stepper prototype reached 90% completion in September 1986. Remaining work needed to achieve a fully operating lithographic system consists of software and some control electronics dealing with wafer handling and lateral/-gap signals and the control of the associated stage drive mechanisms. Using boron nitride X-ray masks, fabricated by the ALO facility, a series of wafer exposures were made to evaluate critical dimension control and overlay alignment. These early exposure tests show overlay errors of 0.1 micron. Factory acceptance tests of the stepper are scheduled for February 1987.

The effort on the high brightness source subcontract was temporarily suspended in January 1986 to redefine the program scope. Work was restarted in October 1986 and is scheduled to be completed within six months. Plans are in progress for installation of the X-ray stepper tool in the VHSIC Phase 2 pilot line at Motorola so that the machine may be characterized and evaluated in a production line setting.

3. Advanced Wafer Imaging System

The Advanced Wafer Imaging System (AWIS) addresses the needs of the VHSIC program for high resolution, high throughput lithography by extending optical lithography beyond its present limitations. The goal of the program is to design a production prototype machine which can produce VHSIC Phase 2 0.5 micron chips of at least one square centimeter area, 0.1 micron alignment accuracy, at a rate of 25 4-inch wafers per hour. The successful completion of the program would provide a cost effective production lithography for VHSIC/VLSI manufacturing.

The AWIS contract was awarded to GCA in October, 1985. The Tropel Division of GCA is supporting the AWIS contract with the design and manufacture of the laser/lens subsystem. The program has been structured into three phases, with Phase 1 currently funded. This phase will provide the integration of the laser/-lens subsystem into a DSW 8000 frame for demonstration of the resolution capability. Optical testing will be done at GCA followed by pilot line testing on the IBM 0.5 micron pilot line at Manassas, Virginia. The remaining two phases of the program will include the manufacture and test of the alignment subsystem, the integration of all the subsystems into the AWIS frame, and then further testing.

During 1986, GCA completed design of the AWIS lens and fabrication of the lens components. Lens assembly is to be completed in January 1987. The DSW frame has been delivered to Tropel for integration of the laser/lens subsystem. GCA is compiling a comprehensive summary of the safety and maintenance requirements for the laser system.

Integration and test of the initial work is planned in early 1987 at GCA by both GCA and IBM. After that, the machine will be installed at Manassas for a 12 month testing program. Detailed comparison is planned between the optical and E-beam lithography techniques for VHSIC production.

V.3   RADIATION HARDENING

1. Status of Phase 1 Hardness Levels

Radiation tests have been performed by the six Phase 1 contractors in order to characterize the tolerance of Phase 1 chips to the five major nuclear and space radiation threats: total dose effects, neutron damage, ionizing dose rate for upset and latchup, ionizing dose rate for survivability, and single-event upset (SEU) produced by alpha particles, protons, and heavy ions. The tests were conducted under Defense Nuclear Agency's (DNA) program on Transient Radiation Effects in Electronics (TREE) in support of the VHSIC Program. DNA's principal objectives in supporting VHSIC have been (1) to insure that the VHSIC Phase 1 radiation hardness requirements and goals are met and (2) to enhance the hardness of selected VHSIC technologies in order to extend radiation tolerances to levels suitable for satellite applications.

All radiation testing during the program was performed in accordance with a DNA test approach that required the use of standard test procedures, the use of common or similar test facilities, and testing to failure, where practical. Test procedures were developed to provide general as well as specific guidelines for testing in each environment without being unnecessarily restrictive or imposing nonessential test requirements that would increase program costs beyond available resources. For example, total dose testing was permitted over a relatively wide range of dose rates to enable use of Co-60 gamma cells at contractor facilities. Tests at low and high military specification temperature extremes (-55°C and +125°C) were not imposed largely because of budgetary constraints. With the exception of total dose and SEU tests performed using contractor-owned Co-60

gamma cells and alpha sources, respectively, all tests were conducted at common Government test facilities in order to minimize source- and spectrum-related variation in test data.

In accordance with DNA's test guidelines, a test plan describing proposed test devices, parameters to be measured and specific test procedures was submitted by each contractor to DNA for review and approval prior to each test.

Although one of the major objectives of this work was characterization of Phase 1 device hardness, much of the total dose test data for some technologies was developed in support of continuing process development and hardening activities and are not necessarily representative of the final VHSIC processes. Also, potential latchup fixes are currently being evaluated for both the CMOS and the bipolar technologies and, if successful, may eventually be incorporated into the main Phase 1 processes. Thus, further improvements in radiation hardness are possible in these areas.

Since only a few fully functional VHSIC chips were available for radiation testing during the program, tests had to be conducted on the most representative samples available. These included partially functional VHSIC chips, macrocells, and test circuits, as well as discrete devices and test structures. None of the VHSIC chips or macrocells evaluated were tested at the 25 MHz maximum clock rate specified for Phase 1 devices. However, some test circuits were evaluated at this frequency. The current hardness capability of each of the eight Phase 1 technologies is summarized in references V.4 and V.5.

2. Other Radiation Hardening Activity

In order to further harden Phase 1 and Phase 2 chips to the levels required systems for various military applications, the VHSIC Program Office has funded the efforts described below. A list of the contractors, contract numbers, and point of contact is included in Appendix II.

a) Motorola - Bulk CMOS

Motorola will radiation harden its bulk CMOS Phase 1 technology to meet space radiation requirements. It will also provide a foundry for radiation hard CMOS. The overall hardness will be demonstrated by redesign (if necessary), fabrication, and testing of the 6K gate array with several different personalizations.

Motorola has demonstrated radiation hardness in test devices by hardening the gate oxide and using a guard band in the field region. This approach to radiation hardening will require modification of the VHSIC Phase 1 design rules. A new field oxide hardening approach will be investigated which will not require any design rule changes.

b) RCA - CMOS Silicon-on-Sapphire

RCA will radiation harden the 1.25 micron CMOS/SOS technology to space radiation levels and provide foundry services for radiation hard CMOS/SOS devices. The radiation hardness will be demonstrated by designing, fabricating,

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and testing a 64K SRAM.

Test chip results indicate that the CMOS/SOS technology will meet the space requirements. The design of an 8K x 8 static RAM began in November 1986. Final RAMS are scheduled to be delivered in April 1988 for government evaluation.

c) National Semiconductor - Bulk CMOS

National Semiconductor will radiation harden its Phase 1 bulk CMOS technology to meet the space radiation requirements and provide foundry services for radiation hard bulk CMOS. The radiation hardness will be demonstrated by redesigning (as required) and radiation testing 64K static RAMs fabricated on the National line and 10K gate array personalizations fabricated on both the National and the Westinghouse pilot lines.

Wafers from a recent run of 64K SRAMs at National Semiconductor on the VHSIC pilot line were tested by Westinghouse and met the total dose requirements for space. Previous results had shown that the CMOS on epitaxial wafers did not latch up under gamma pulse irradiation. The new contract will make additional total dose enhancements and harden the RAM and the 10K gate array against single particle induced upsets from cosmic rays.

d) Hughes Aircraft - CMOS Silicon-on-Sapphire

Hughes has radiation hardened its CMOS/SOS Phase 1 technology and will provide radiation hard CMOS/SOS foundry services for the space radiation levels. In addition to a custom VHSIC design capability Hughes plans to offer gate arrays in CMOS/SOS by early 1987.

e) Texas Instruments - STL Bipolar

Under a new contract started in October 1986, T.I. will eliminate dose rate induced latch up and increase the dose rate induced upset threshold in its Phase 1 STL bipolar technology and provide a foundry for radiation hard VHSIC bipolar chips. The latching macrocell will be identified. Then a set of layout/processing design rules to eliminate latch up will be developed and verified. The immunity of Array Controller/Sequencer (ACS) chips will be measured as a demonstration of the hardening results.

f) TRW - 3D Bipolar

Under a new contract started in October 1986, TRW will harden its 3D bipolar Phase 1 technology against radiation induced latch up. It will investigate design and layout changes using test chips fabricated on p/p+ epitaxial material and demonstrate the latch up immunity on the CAM chip which currently latches under gamma pulse irradiation.

g. Booz-Allen - Electromagnetic Effects

The goal of this program is to improve the survivability of VHSIC chips in a severe electromagnetic environment. Booz-Allen will review the varieties of

input/output protection used on VHSIC/VLSI chips for electrostatic discharge (ESD) protection. It will analyze and select those approaches which will offer the most chip protection against other electromagnetic threats, including EMP and SGEMP.

This program started in September 1986. A survey of the state of the art in ESD protection is underway.

V.4   OTHER CURRENT PROJECTS (Active in 1986)

The Phase 3 programs which have been active in 1986 include 42 projects or tasks whose starting dates range from 1981 through 1986. Some of these are continuations of early Phase 3 tasks. They are being carried out by 24 organizations from industry, research institutes and government laboratories. The technical areas are being investigated: (1) materials and processes, (2) packaging technology, and (3) reliability and testability. These projects are identified and summarized below. Further information on these projects is contained in VHSIC Briefs, May 1986 (reference V.6). See Appendix II for contract numbers and key personnel.

1. Materials and Processing

    a. Hughes Research - Silicon On Sapphire

        There are three major goals of this program by Hughes Aircraft Company and its major subcontractor, Union Carbide, namely:

        o optimization of the recrystalization processes for fabricating silicon-on-sapphire (SOS) wafers,

        o fabrication of very thin (0.3 micrometer) SOS wafers on a pilot line basis,

        o identification of the best available diagnostic techniques for characterizing the SOS starting material.

        The recrystalization techniques that have been employed for improving the SOS materials are solid phase epitaxy and regrowth (SPEAR) and double solid phase epitaxy (DSPE).

        During the period November 1984 to July 1985, 50 wafers were processed in three separate submicrometer CMOS device lots for demonstrating improved performance. Although in all cases a large improvement in overall crystallinity was achieved by recrystalization, the reproducibility was found to be strongly dependent on SOS material characteristics.

        In order to optimize and further narrow the recrystalization parameters for achieving better reproducibility, a study of the implant parameters for both SPEAR and DSPE was initiated. Excellent correlation was obtained between the

experimental data and modeling results for optimizing the SPEAR process.

In summary, Hughes has performed the solid phase epitaxial process optimization and is now in the process of transferring the technology to Union Carbide. The work will continue until the transfer is complete and the results documented. Project funds were terminated as of 1 October 1985.

b) Westinghouse – Magnetic Czochralski Silicon Growth

The goals of this program are twofold: (1) to develop a process for providing the highest quality silicon currently available to the VHSIC program and (2) to transfer this process to a commercial vendor who will supply wafers in quantity to VHSIC contractors. The major problem to be overcome is the control of impurities in the substrates. The approach selected is the Magnetic Czochralski technique.

A crystal puller was constructed with an axially symmetric field. The system was fully characterized at a number of different growth conditions. The results showed that the axially symmetric field does not provide uniform oxygen content across the wafer.

This program has been terminated and a final report is being prepared.

c. Lawrence Livermore Laboratory – Laser Pantography

The goal of the Laser Pantography (LP) Project is to develop an automated facility for fast fabrication of high performance digital electronic systems.

The Laser Pantography project was established to:

o   support fabrication of wafer scale integrated (WSI) systems on silicon substrates,

o   fabricate and test WSI systems in less than 100 hours,

o   completely automate these processes,

o   demonstrate the capabilities of such a system.

In support of these objectives, three tasks are being carried out. Under Task I, a 1000 gate array circuit consisting of five 16-stage shift registers and a 16-stage counter has been fabricated and tested to be fully functional. Six pieces were delivered to DoD as scheduled. Work continues on the CAD to support this task.

Under Task II, laser planarization of silver, gold, and aluminum thin films has been demonstrated over a 3 inch wafer.

Under Task III, 2 kW of power has been successfully generated on the front surface of a silicon wafer and removed from the rear surface with only a 22 degree worst case temperature rise on the wafer (the cooling water rise was six degrees). In addition, the ability to write doped polysilicon lines from an

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attached silicon chip down a beveled edge to a silicon substrate has been success-
fully demonstrated.

2. Packaging Technology

a) Martin Marietta - High Density Multilayer Package

The objective of this program is to develop a family of hermetic chip
packages suitable for all Phase 1 VHSIC chips. The package family will be a
perimeter style ceramic chip carrier with terminals on 20 mil centers for surface
mounting. The 264 lead package will be tooled as representative of the family
and demonstrated. Provisions will be made for socketing, and second level
mounting will be demonstrated. The packages will be capable of using either tape
or wire chip interconnect.

The family of 20 mil pitch perimeter chip packages is being coordinated
with JEDEC via Martin Marietta and Hughes Aircraft, and final standardization is
expected. The 264 I/O package was designed by Martin Marietta and fabricated
by Ceramic Systems, the package subcontract vendor. A connect/carrier was
developed and supplied by Wells Electric.

b) Hughes Aircraft - Printed Wiring Boards

The objective of this program is to develop printed wiring boards (PWB)
which have a significantly lower dielectric constant and loss tangent than current
printed wiring boards.

The developmental PWBs will also be required to have (a) a coefficient of
thermal expansion about equal to that of the aluminum oxide used in leadless chip
carriers, (b) low moisture absorption, (c) low dissipation factor, (d) better high
temperature strength than epoxy PWBs, (e) good hole drilling characteristics, and
(f) cost effectiveness.

The contractor has reviewed a number of candidate resin formulations such
as a low dielectric constant resin system recently developed by Westinghouse
under another contract. The remaining work will be to achieve as low a dielec-
tric constant as possible while providing a high enough T_g to ensure the integrity
of plated-through holes during soldering and temperature cycling.

c) Honeywell - High Density Multilayer Package

The objective of this program is to develop a family of hermetic chip
packages suitable for all Phase 1 VHSIC chips. The result is a family of pin grid
array (PGA) ceramic packages with pins on a 50 mil grid. The program has been
completed and a final report is being distributed. The program was successful in
defining a family of PGA packages with the number of I/O's ranging from 120 to
480 leads. Chip-to-package interconnection was demonstrated using a thermal test
chip and the Phase 1 sequencer chip with tape automated bonding solder reflow.
A 240 lead demonstration package was fabricated and delivered.

d) Hughes - High Density Multilayer Package

The objective of this program is to develop a family of hermetic chip packages suitable for all Phase 1 VHSIC chips. The package family will be a perimeter style ceramic chip carrier with terminals on 20 mil centers for surface mounting.

A family of 20 mil pitch perimeter chip packages was defined and coordinated with standardization efforts of the JEDEC JC-11 Committee. The number of I/O's for the family of packages range from 108 to 308 leads. Bourns packages (264 I/O) utilizing thick film technology were evaluated by Hughes and delivered to LABCOM. Co-fired packages from Tektronix with 264 I/O were also evaluated by Hughes and transmitted to LABCOM. Chip carrier sockets were developed and delivery was made by AMP Corporation. Tab interconnects from 3M were used for inner-lead and outer-lead bonding studies.

e) VHSIC Packaging Workshop

A VHSIC Packaging Workshop was held at the Naval Surface Weapons Center on June 5-6, 1985. See reference V.7.

3. Reliability and Testability

a) Research Triangle Institute - Chip Testability

The Research Triangle Institute is tasked to perform a technical evaluation of the VHSIC Phase 1 demonstration test plans. This evaluation is to be accomplished by (1) reviewing all VHSIC Phase 1 test plans dealing with the demonstration of chip testability and fault tolerance, (2) observing the Phase 1 chip/brassboard demonstrations, and (3) analyzing each test plan and demonstration for adequacy and appropriateness.

On 1 May 1984, the first Phase 1 chip/brassboard demonstration was conducted by the Federal Systems Division of IBM, Manassas, Virginia. The technical evaluation results indicate that the IBM chip/brassboard test plan evaluation methods are appropriate and adequate to verify chip testability and fault tolerance. Technical evaluation of the IBM Phase 1 demonstration is reported in reference V.8. An evaluation of the results of the TRW testability demonstration are reported in reference V.9.

b) GenRad - Advanced High Speed Test System

The objective of this program is to establish the capability to test VHSIC and VLSI devices using an enhanced commercially available automated microcircuit test equipment (AMTE) system. This equipment will be used for precise parametric measurements and functional testing of complex integrated circuits with pin counts in excess of 200 and speeds of 40 MHz.

The standard GR-18 test system was successfully demonstrated at GenRad (Milpitas, California) to personnel from Wright-Patterson AFB, Rome Air Develop-

ment Center, and Crane Naval Weapons Support Center on 20-22 August 1985. The system was then shipped to RADC at Griffiss AFB, NY, where it is now installed.

The capability to test complex IC devices containing up to 288 I/O pins was demonstrated at RADC, utilizing the full test capability of this GR-18 test system. Future enhancements of the GR-18 test system will be developed at GenRad over the next year.

c) Harris - Tester Independent Support Software System

The objective of this effort is to develop a system for the automated generation and maintenance of electrical test specifications and test programs for VHSIC and VLSI devices. This will be accomplished through the development of a Tester Independent Support Software System (TISSS). This system will provide a capability for the government to develop and maintain high reliability specifications in a standardized, transportable, and computer-accessible format and to automatically generate test programs.

The TISSS program was structured in two phases: a 6 month competitive design phase (Phase 1), and a 28 month follow-on implementation phase (Phase 2).

Phase 1 was successfully completed on June 1985 by both PCA and Harris. Phase 2 was awarded to Harris in September 1985. A Critical Design Review for software development was held by the Government at Harris in September 1986. Harris has now begun code development and unit test of the software. A review of TISSS for industry was held in Phoenix in October 1986. The TISSS program was reorganized during December 1986 because of delays in the delivery of the VHDL simulator which was to have been provided to the contractor in June 1986. The revised date for delivery of the simulator is February 1987. Therefore, the development of the modeling subsystem of TISSS which incorporates the simulator has been delayed by approximately one year. The reprogramming has also eliminated the planned beta site efforts.

Several test equipment manufacturers have requested technical documentation in order to begin development of TISSS postprocessors for their line of equipments. This documentation is expected to be available in March 1987 and will be provided along with software specifications and interface requirements. The TISSS concept is being extended to support printed circuit board and module design for the Computer Aided Logistics Support Office and the Modular Avionics System Architecture Office.

d) Honeywell - Maintenance Concepts For VHSIC

The objectives of this effort are to (1) identify the unique diagnostic and maintenance aspects of systems using VHSIC technology and (2) develop guidelines to structure maintenance concepts and control and facilitate the maintainability design of VHSIC-based systems. Specifically, the impact of VHSIC technology on field maintenance (both the current three levels of maintenance and advanced on-and-off-equipment maintenance concepts) will be evaluated with respect to testability and repairability of the system, special test and support equipment required, special handling and packaging requirements, shelf life and storage

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requirements, and the integration of VHSIC diagnostic capabilities with system diagnostics.

The status of current VHSIC technology development programs has been reviewed. VHSIC vendor plans for chip maintainability, repairability, and diagnostics are being collected and reviewed. Current Air Force maintenance system structure and repair capabilities are being reviewed and evaluated as a result of personal contacts and visits to maintenance facilities. The scope and structure of the maintainability design guidelines to be developed have been defined. Packaging, transport packaging, and electrostatic discharge sensitivity are also being investigated. The candidate insertion project for applying the guidelines has been identified as the AN/ALQ-131 program.

e) General Dynamics - VHSIC Impact On System Reliability

The objective is to perform an assessment of the impact of VHSIC technology on system reliability and system reliability design procedures, including the incorporation of fault tolerance. This effort will produce guidelines which can be used by both the Air Force and contractors for the reliable design of VHSIC-based systems. The approach to be taken will include an investigation of the effect of VHSIC circuits on system reliability and an investigation of chip-level and brassboard-level fault tolerant design techniques.

Four brassboard/breadboard VHSIC designs have been selected for detailed study:

Multimode Fire and Forget Electronics (T.I.)
AN/ALQ-131 (TRW)
Programmable Signal Processor (Westinghouse)
Common Signal Processor (IBM)

Contracts with the government program offices and the contractors have been established and data is being collected. That data will be compared to data associated with contemporary non-VHSIC designs. After some final fine-tuning, the data and the resultant comparisons will serve as the basis of this study's conclusions.

f) Vanzetti Systems - Non-Destructive Bond Testing

This effort is one of two 24 month investigations to develop a method for testing the quality of metallurgical bonds formed in the process of connecting VLSI/VHSIC chips to their packages by means of tape automated bonding (TAB). The end item of this program will be a report detailing the test method developed.

This program will generate a test method using infrared thermal non-destructive techniques that will be submitted for coordination and implementation in MIL-STD-883.

The effort will also develop a non-destructive evaluation technique with the necessary resolution to assess these chip and package metallurgical bond sites and will establish the parameters that distinguish an acceptable bond from a defective

one. The contract was awarded and effort begun in April 1986.

  g) Sonoscan - Non-Destructive Package Screening

  This effort is one of two 24 month investigations (see item 3(f) above) to develop a method for testing the quality of metallurgical bonds formed in the process of connecting VLSI/VHSIC chips to their packages by means of tape automated bonding (TAB). The end item of this program will be a report detailing the test method developed.

  The program will generate a test method using acoustic non-destructive techniques that will be submitted for coordination and implementation in MIL-STD-883. The effort will also develop a non-destructive evaluation technique with the necessary resolution to assess the package metallurgical bonding and will establish the parameters that distinguish an acceptable bond from a defective one. The contract was awarded and effort begun in April 1986.

V.5   Prior Projects

  The initial Phase 3 program consisted of 59 projects or tasks, most of which began in 1980. They were carried out by 50 performing organizations, which included both large and small industrial contractors, universities, research institutes, and three government laboratories. The technical categories covered by the projects include (1) architecture studies (devices and systems), (2) lithography, (3) other processing techniques, (4) design automation, (5) materials research and characterization, (6) device technology, (7) hybrid packaging technology, and (8) reliability, testing, characterization, and standardization. Appendix II lists the completed Phase 3 project titles, contract numbers, performing organizations, and (if available) final report DTIC numbers. Technical summaries of these projects can be found in VHSIC Briefs (Phase 3 Projects), references V.10 and V.11.

SECTION VI

MANAGEMENT

VI.1   TECHNOLOGY TRANSFER

The VHSIC Program Office, from the outset, recognized that the transfer of
VHSIC technology and products to both the DOD contractor community and DOD
acquisition managers is essential for program success. It also recognized that
historically this had been a difficult task to achieve. Novel approaches were
needed to ensure that system designers would not only have access to VHSIC
technology but also to VHSIC software and devices as quickly as they became
available. Part of this effort is being carried out in the military weapon system
technology insertion projects. An additional part of this effort is the VHSIC
training and information program.

A major source of information for the defense community is and will continue
to be the Defense Technical Information Center (DTIC). DTIC has on file well
over 1000 documents relative to VHSIC and VHSIC related technology. DTIC is
accessible to qualified users, including U.S. Government agencies, their contrac-
tors, subcontractors, and potential contractors who have established a "need to
know" at DTIC.

The VHSIC training program has been structured as a two part effort which
began in January 1984.

        Part I: 1984-1986   Awareness and Initial Training

        Part II: 1986-1988   Extended Training and Policy Development

                PART I: Awareness and Initial Training

The objective of Part I of the VHSIC Training and Policy Program has been to
provide for initial education and training during which the following has been
accomplished:

o   system managers and senior engineers have been made aware of
        the VHSIC products and design technologies being developed,

o   working level engineers have been trained in the design of
        systems using VHSIC products through hands-on design work-
        shops.

1. Workshops

The primary techniques for accomplishing the Part I objectives have been
regional workshops, conferences, presentations, and brochures. For the more

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technical hands-on workshops special software has been developed for using VHSIC design tools and detailed technical reference material has been prepared in the form of application notes, performance data sheets, and text books.

VHSIC Application Workshops have been organized and held throughout the country on a regional basis. The workshops provide comprehensive training and education in VHSIC technology for defense contractor personnel for the purpose of accelerating the application of VHSIC technology in military electronics. More than 3000 engineers and technical managers have attended them. A list of the workshops held is shown below.

The scope and depth of coverage of VHSIC technology at these workshops have enabled each attendee to evaluate the feasibility of using VHSIC technology in specific military system applications. Attendees are given the opportunity to present both application and work-related problems which are discussed by the group in terms of how VHSIC can be applied. The attendees are provided approximately three days of instruction using text material which they take with them for future use in electronic design and interface with the VHSIC community.

The instructional material includes:

o   Student Guide - a compilation of VHSIC design data and the chip architectures used as the text material by the workshop instructors,

o   VHSIC Specification Guide - an abbreviated version of all of the VHSIC chip specifications (reference II.45),

o   Interface Reference Guide - a collection of technical and management information about ICs, Computer Aided Design (CAD) availability, documents available, as well as key government and industry personnel.

A number of similar workshops have been held for DOD and other government personnel at such in-house facilities as the Naval Ocean Systems Center (San Diego), the Naval Weapon Center (China Lake), Eglin Air Force Base (Florida) and NASA's Johnson Spaceflight Center (Houston).

VHSIC APPLICATIONS WORKSHOPS

1984 - 1986

SITE	DATE
1 Naval Ocean Systems Center, San Diego, CA	March 1984
2 Lockheed/Georgia Tech., Atlanta, GA	April 1984
3 Environment Research Institute of Michigan, Ann Arbor, MI	May 1984

4	Northrop Corp., Anaheim, CA	May 1984
5	Grumman Aerospace, Bethpage, NY	June 1984
6	E-Systems, Dallas, TX	June 1984
7	Lockheed Missiles and Space Co., San Francisco, CA	July 1984
8	Colorado/Wyoming Chapter of the American Defense Preparedness Association	July 1984
9	Johns Hopkins U./APL, Laurel, MD	August 1984
10	Litton Data Systems, Los Angeles, CA	August 1984
11	Mitre Corp./Raytheon Co., Boston, MA	October 1984
12	Gould, Inc., Chicago, IL	October 1984
13	NASA, Johnson Space Center, Houston, TX	November 1984
14	Martin Marietta, Orlando, FL	November 1984
15	Naval Weapons Center, China Lake, CA	January 1985
16	Boeing Aerospace Co., Seattle, WA	February 1985
17	McDonnell Douglas, St. Louis, MO	March 1985
18	Sanders Assoc., Nashua, NH	April 1985
19	Johns Hopkins U., APL, Laurel, MD	June 1985
20	RCA, Princeton, NJ	September 1985
21	United Technologies Microelectronics Center Colorado Springs, CO	October 1985
22	US Army LABCOM, Ft. Monmouth, NJ	October 1985
23	Ford Aerospace, Newport Beach, CA	October 1985
24	Rockwell, Anaheim, CA	November 1985
25	Eglin AFB, FL	March 1986
26	General Dynamics, San Diego, CA	April 1986
27	Lockheed, Plainfield, NJ	May 1986
28	Wright-Patterson AFB, OH	June 1986

29 Johns Hopkins University/APL, Laurel, MD   August 1986

30 Rockwell International, Anaheim, CA   November 1986

A major follow-on effort to the Applications Workshops was developed by the Johns Hopkins University Applied Physics Laboratory and was initiated in June 1985. It is called "Applications II" and is intended for those system designers who have attended the regional workshops. It builds on their knowledge from earlier workshops and concentrates exclusively on how to design electronic components using VHSIC products. This two day training program allows hands-- on use of some of the CAD tools developed for the VHSIC Program. Four Applications II workshops were held during the summer of 1985. A further extension of these workshops called Applications III was held by JHU/APL in October 1986. See reference VI.1

2. Conferences

Each year, normally in December, the VHSIC Program Office holds a VHSIC Conference to which a broad representation of defense industry managers are invited. These three day meetings are structured to present industry with an updated report on the status of the VHSIC program and an indication of the directions and plans for the next year. The meeting is attended by about 400 people each year. In addition to discussions of VHSIC technology issues, the concerns of system designers who are not VHSIC contractors are openly discussed. See references VI.2 - VI.6.

3. Brochures

In order to bring an awareness of the VHSIC program to as wide a group of industrial and DOD people as possible, a semi-technical brochure has been prepared and distributed. The brochure describes the purpose, the content and the goal of the VHSIC program. It stresses the potential for widespread application of the technology and hence the need for widespread participation of system developers in using the technology. Approximately 5,000 of these brochures have been printed and distributed throughout the defense community.

PART II: Extended Training and Policy Development

As a result of the Awareness and Initial Training efforts described as PART I, a number of adjunct activities are being undertaken. Applications Workshop efforts are being followed up with increasingly detailed technical design information and data. As they reach the detailed design of specific systems, design level engineers need both tools and data which will allow them to determine specifications, performance, cost, configuration, and reliability of a system and its components. A larger number of people at both the technical and the managerial level are being made aware of the content, the products and the advantages of VHSIC technology. Information generated by the VHSIC program has become sufficiently voluminous and complex that a formal system is being devised to organize it for most effective use by managers and engineers.

The following specific efforts have been or are being taken:

1. VHSIC Seminars/Courses:

o A one hour multi-media briefing has been produced for use at Service schools, defense contractor facilities, and System Program Offices. This briefing is designed to serve both as an introduction to VHSIC and a means to provide information on gaining access to VHSIC design data.

o A three hour multi-media presentation is being produced for middle managers in both industry and in the government which covers more technical detail and serves to suggest specific areas of application that could be served by VHSIC technology. This presentation is scheduled to be available in early 1987.

o A two day technical seminar on VHSIC design software has been organized and held. The seminar covers software availability and how it can be used. As part of this effort, a rule based Format Translator is being developed which provides for translation between various VHSIC software design tools and selected engineering graphic work stations. The translator will enable a system designer to learn how to put VHSIC design tools to use in solving his particular design problems.

o A two day seminar on VHSIC signal processing was held at the Naval Post Graduate School in Monterey, CA. This seminar highlighted the increase in signal processing throughput and system performance improvements that can be gained from VHSIC technology. See reference VI.7.

o As a result of the impetus provided by VHSIC education programs a number of independently sponsored courses are being offered which focus on specific areas of VHSIC design methodology. One course on the VHSIC Hardware Design Language is offered by the Air Force Institute of Technology (AFIT). A second course is being scheduled by the Johns Hopkins Applied Physics Laboratory on the use of VHSIC in the design of high speed parallel processors.

2. On-Site Training Kit/VHSIC Text Book

In order to reach a much wider group of design level engineers, an On-Site Training Kit is being developed. The kit consists of much of the written material distributed at the Applications Workshops but with the tests expanded so that the kit may be used independently. In addition, a textbook has been prepared which covers the engineering details of how to design a system using VHSIC ICs. See references VI.8 and VI.9.

3. VHSIC Data Base

The management and technical data base being generated by VHSIC Program efforts is very large. A centralized information system is in development to organize this data and provide access to it by the entire defense community.

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This data base is an on-line system that will be available 24 hours a day, seven days a week. With the relational data base presently residing on a DEC VAX 11/780 computer, the data base structure will consist of the following eight areas:

- o Personnel
- o Integrated Circuits
- o Applications
- o Technical Documents
- o Projects and Contracts
- o Briefing Materials
- o Software Tools
- o Training

The data base is menu driven and highly interactive. The complete data base is expected to be operational in early 1987 at which time the most up-to-date versions of VHSIC IC specifications will be accessible, as well as current chip availability and cost data.

VI.2   Technology Security

The enhanced performance of systems made possible by VHSIC and the comparative military advantage they provide make program security a matter of critical importance. VHSIC devices have been placed on the US Munitions list and are subject to International Traffic in Arms Regulations (ITAR). Availability and dissemination of all documentation is regulated accordingly.

Two documents have been prepared and issued that deal with the security aspects of VHSIC technology – the VHSIC Program Security Classification Guide (DoD Instruction 5010.75) and the VHSIC Technology Security Program (DoD Instruction 5230.26) which are in Appendix I as references VI.11 and VI.12.

The Classification Guide authorizes controls of VHSIC devices and technology by classification, International Traffic and Arms Regulations (ITAR), Export Administration Regulations (EAR), or contractor certification. Inasmuch as both the ITAR of the Department of State and the EAR of the Department of Commerce apply to VHSIC, the VHSIC Program Office has the responsibility to ensure consistent implementation of security classification guidelines.

Since the ultimate goal and much of the activity is the insertion of the technology into military weapon systems, the scope of VHSIC information that is sensitive, even if unclassified, is widespread. In addition to design and processing data, there is a plethora of hardware or module information related to various weapon systems or military applications. This information constitutes technical data which may be unclassified but requires a validated license under the ITAR for release to another country. A procedure had to be established to protect this information from release to unauthorized users while ensuring easy access to it by authorized users. Hence, the Security Program was developed to minimize reliance on classification and maximize the use of existing industrial practices.

In order to ensure that the requirements of the Security Program are implemented in existing and new contracts, steps have been taken to effect changes to the Federal Acquisition Regulations (FAR). These changes are being reviewed by the Defense Acquisition Council at this time.

Concurrently, a procedure for sharing VHSIC technology with our Allies has been developed by the VHSIC Program Office and proposed to OSD (Policy) as a basis for an overall DoD VHSIC Technology export policy. This procedure assigns a release category to each element of the VHSIC program. A draft policy statement incorporating this release procedure has also been prepared and is being reviewed. It is expected that a DoD VHSIC technology export policy will soon be issued.

APPENDIX I

REFERENCES

Section I   Introduction

1.1   General Electric VHSIC Program Definition (Phase O) Final Technical Report, 03/07/80-12/12/80, Contract DAAK20-80-C-0255

I.2   Honeywell VHSIC Program Definition (Phase O) Final Technical Report, 03/15/80-12/15/80, Contract F36615-80-C-1124, DTIC No. AD-B065-779

I.3   Hughes VHSIC Program Definition (Phase O) Final Technical Report, 03/01/80-12/01/80, Contract DAAK20-80-C-0256

I.4   IBM VHSIC Program Definition (Phase O) Final Technical Report, 09/09/80-01/09/81, Contract N00039-80-C-0284

I.5   Raytheon VHSIC Program Definition (Phase O) Final Technical Report, 03/15/80-01/15/81, Contract F33615-79-C-1853, DTIC No. AD-B062-876

I.6   Rockwell VHSIC Program Definition (Phase O) Final Technical Report, 04/07/80-03/31/81, Contract DAAK20-80-C-0256

I.7   Texas Instruments VHSIC Program Definition (Phase O) Final Technical Report, 03/15/80-12/05/80, Contract F33615-80-C-1123

I.8   TRW VHSIC Program Definition (Phase O) Final Technical Report, 03/01/80-04/01/81, Contract F33615-80-C-1123

I.9   Westinghouse VHSIC Program Definition (Phase O) Final Technical Report, 03/01/80-06/01/81, Contract N00039-80-C-0283

I.10   L.R. Weisberg and L.W. Sumney, The New DoD Program on Very High Speed Integrated (VHSI) Circuits, Proceedings of the Government Microelectronics Circuits Conference (GOMAC), November 1978

I.11   R.M. Davis, The DoD Initiative in Integrated Circuits, Computer, pp. 74-79, July 1979

I.12   L.W. Sumney, VLSI With a Vengeance, IEEE Spectrum, pp. 24-27, April 1980

I.13   Rhea, J., VHSIC: Advanced Components For a New Generation of Weapons Systems, International Defense Review,   pp. 887-890, June 1980

I.14   Barbe, D.F., VHSIC Systems and Technology, Computer, pp. 13-22, February 1981

I.15   Klass, P.J. and Elson, B.M., Technical Survey: Very High Speed Integrated Circuits, Aviation Week and Space Technology, pp. 48-85, 16 February 1981

I.16   Martin, J., Very High Speed Integrated Circuits - Into the Second
        Generation, Military Electronics/Countermeasures, December 1981-April
        1982 (in five parts)

I.17   Sumney, L.W., VHSIC: A Status Report, IEEE Spectrum, pp. 34-39,
        December 1982

I.18   Cohen, E.D., The Very High Speed Integrated Circuits Program,
        Presentation by United States at Nato North Atlantic Council, Defense
        Research Group Meeting, Brussels, Belgium, September 1983

I.19   Klass, P.J. and Elson, B.M., Technical Survey: VHSIC Chips Emerge,
        Aviation Week and Space Technology, pp. 46-65, July 1984

I.20   Weiss, R., The Hardware Language Devised for VHSIC is Poised for
        Takeoff, Electronic Design, pp. 67-76, January 1985

I.21   Allan, R., Technology Report: VHSIC, Electronic Design, pp. 95-114,
        April 1985

I.22   Castellano, R.N., The VHSIC Program: A Technology Impact Report
        Analyzing the VHSIC Program Scope, Status, and Impact on the Commer-
        cial IC Market, 1986, Electronic Trend Publications, Cupertino, CA
        95014. Library of Congress Catalog No. 86-080562, ISBN No. 0-914405-
        14-4.

Section II   Phase 1

II.1   Honeywell VHSIC Phase 1 Interim Technical Report #1, 04/01/81-09/30/-
        81, Contract F33615-81-C-1527, DTIC No. AD-B066-012

II.2   Honeywell VHSIC Phase 1 Interim Technical Report #2, 10/01/81-
        03/31/82, Contract F33615-81-C-1527, DTIC No. AD-B066-012

II.3   Honeywell VHSIC Phase 1 Interim Technical Report #3, 04/01/82-
        09/30/82, Contract F33615-81-C-1527, DTIC No. AD-B070-598

II.4   Honeywell VHSIC Phase 1 Interim Technical Report #4, 10/01/82-03/31/-
        83, Contract F33615-81-C-1527, DTIC No. AD-B074-983

II.5   Honeywell VHSIC Phase 1 Interim Technical Report #5, 04/01/83-09/30/-
        83, Contract F33615-81-C-1527, DTIC No. AD-B078-931

II.6   Honeywell VHSIC Phase 1 Interim Technical Report #6, 10/10/83-03/31/-
        84, Contract F33615-81-C-1527, DTIC No. AD-B083-840

II.7   Honeywell VHSIC Phase 1 Interim Technical Report #7, 04/01/84-09/30/-
        84, Contract F33615-81-C-1527, DTIC NO. AD-B074-9873

II.8   Honeywell VHSIC Phase 1 Interim Technical Report #8, 10/01/84-03/31/-
        85, Contract F33615-81-C-1527, DTIC No. AD-B096-015L

II.9   Hughes VHSIC Phase 1 Interim Technical Report #1, 05/01/81-10/31/81,
        Contract DAAK20-81-C-0383

II.10   Hughes VHSIC Phase 1 Interim Technical Report #2, 11/01/81-04/30/82,
        Contract DAAK20-81-C-0383 DTIC No. AD-B072-716-717,718

II.11   Hughes VHSIC Phase 1 Interim Technical Report #3, 05/01/82-10/01/82,
        Contract DAAK20-81-C-0383, DTIC No. AD-B072-873

II.12   Hughes VHSIC Phase 1 Interim Technical Report #4, 04/30/83-11/01/83,
        Contract DAAK20-81-C-0383, DTIC No. AD-B081-393

II.13   Hughes VHSIC Phase 1 Interim Technical Report #5, 11/01/83-04/30/84,
        Contract DAAK20-81-C-0383, DTIC No. AD-B088-185L

II.14   Hughes VHSIC Phase 1 Interim Technical Report #6, 05/01/84-10/31/84,
        Contract DAAK20-81-C-0383, DTIC No. AD-B097-450L

II.15   IBM VHSIC Phase 1 Interim Technical Report #1, 05/01/81-11/01/81,
        Contract N00039-81-C-0416

II.16   IBM VHSIC Phase 1 Interim Technical Report #2, 11/01/81-04/30/82,
        Contract N00039-81-C-0416, DTIC No. AD-B068-144

II.17   IBM VHSIC Phase 1 Interim Technical Report #3, 05/01/82-10/31/82,
        Contract N00039-81-C-0416, DTIC No. AD-B071-094

II.18   IBM VHSIC Phase 1 Interim Technical Report #4, 11/02/82-04/30/83,
        Contract N00039-81-C-0416, DTIC No. AD-B075-949

II.19   IBM VHSIC Phase 1 Interim Technical Report #5,   05/01/83-10/31/83,
        Contract N00039-81-C-0416, DTIC No. AD-B080-324

II.20   IBM VHSIC Phase Final Technical Report, 05/01/81-04/30/84, Contract
        N00039-81-C-0416, DTIC No. AD-B091-279

II.21   Texas Instruments VHSIC Phase 1 Interim Technical Report #1, 05/01/8-
        1-10/31/81, Contract DAAK20-81-C-0382, DTIC No. AD-B068-144

II.22   Texas Instruments VHSIC Phase 1 Interim Technical Report #2,
        11/01/81-04/30/82, Contract DAAK20-81-C-0382, DTIC No. AD-B067-794

II.23   Texas Instruments VHSIC Phase 1 Interim Technical Report #3,-
        05/01/82-10/31/82, Contract DAAK20-81-C-0382, DTIC No. AD-B074-361

II.24   Texas Instruments VHSIC Phase 1 Interim Technical Report #4,-
        11/01/82-05/31/83, Contract DAAK20-81-C-0382, DTIC No. AD-B074-361

II.25   TRW VHSIC Phase 1 Interim Technical Report #1, 05/01/81-11/02/81, Contract N00039-81-C-0414

II.26   TRW VHSIC Phase 1 Interim Technical Report #2, 11/03/81-05/03/82, Contract N00039-81-C-0414, DTIC No. AD-B069-021

II.27   TRW VHSIC Phase 1 Interim Technical Report #3, 05/03/82-11/01/82, Contract N00039-81-C-0414, DTIC No. AD-B073-344

II.28   TRW VHSIC Phase 1 Interim Technical Report #4, 11/01/82-05/01/83, Contract N00039-81-C-0414, DTIC No. AD-B077-743

II.29   TRW VHSIC Phase 1 Interim Technical Report #5, 05/01/83-11/30/83, Contract N00039-81-C-0414, DTIC No. AD-B087-777

II.30   TRW VHSIC Phase 1 Interim Technical Report #6, 12/01/83-05/30/84, Contract N00039-81-C-0414, DTIC No. AD-B091-686

II.31   Westinghouse VHSIC Phase 1 Interim Technical Report #1, 05/01/81--11/30/81, Contract F33615-81-C-1532, DTIC No. AD-B085-114

II.32   Westinghouse VHSIC Phase 1 Interim Technical Report #2, 11/01/81--05/31/82, Contract F33615-81-C-1532, DTIC No. AD-B085-115

II.33   Westinghouse VHSIC Phase 1 Interim Technical Report #3, 05/01/82--11/30/82, Contract F33615-81-C-1532, DTIC No. AD-B085-116

II.34   Westinghouse VHSIC Phase 1 Interim Technical Report #4, 11/01/82--05/31/83, Contract F33615-81-C-1532, DTIC No. AD-B085-117

II.35   Westinghouse VHSIC Phase 1 Interim Technical Report #5, 06/01/81--11/30/83, Contract F33615-81-C-1532, DTIC No. AD-B085-118

II.36   Westinghouse VHSIC Phase 1 Interim Technical Report #6, 06/01/84--10/31/84, Contract F33615-81-C-1532,

II.37   Proceedings of the 1985 VHSIC/VLSI Qualification Workshop, Vail, Colorado, September 18-20, 1985, Palisades Institute for Research Services

II.38   Proceedings of the 1986 VHSIC/VLSI Qualification Workshop, Vail, Colorado, September 9-12, 1986, Palisades Institute for Research Services

II.39   IBM VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-260

II.40   Honeywell VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-259

II.41   Hughes VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-255

II.42 Texas Instruments VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-258

II.43 TRW VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-256

II.44 Westinghouse VHSIC Phase 1 Chip Set Specification Handbook OUSDRE, January 1984, DTIC No. AD-B085-257

II.45 VHSIC Specification Reference Guide, VHSIC Applications Workshop material, Revised July 1, 1985, DTIC No. AD-B088-097 (Supersedes AD-B082-891)

II.46 IBM VHSIC Signal Processing Element (SPE) Chip Specification, Version 2.5, 9/15/86

II.47 IBM VHSIC CMAC Chip Specification (Final Chip and Macro Specification) 5/1/84, Contract N00039-81-C-0416

Section IV   Phase 2

IV.1 AT&T VHSIC Submicrometer Program Definition (Phase O'),Final Technical Report, 08/01/83-02/28/84, Contract DAAK20-83-C-0415

IV.2 Harris VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-03/01/84, Contract F33615-83-C-1012, DTIC NO. AD-B094-298L

IV.3 Honeywell VHSIC Submicrometer Program Defn. (Phase O'), Final Technical Report, 08/01/83-02/28/84, Contract F33615-83-C-1103, DTIC No. AD-B093-706,707

IV.4 Hughes VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-01/31/84, Contract DAAK20-83-C-0414, DTIC No. AD-B090-450L, 459

IV.5 IBM VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-02/28/84, Contract N00039-C-83-0638

IV.6 RCA VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-02/28/84, Contract N00039-C-83-0639

IV.7 Texas Instruments VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-02/28/84, Contract DAAK20-83-C-0413, DTIC NO. AD-B089-403L

IV.8 TRW VHSIC Submicrometer Program Definition (Phase O'), Final Technical Report, 08/01/83-01/31/84, Contract N00039-83-C-6040

IV.9 Westinghouse VHSIC Submicrometer Program Def. (Phase O'), Final Technical Report, 08/01/83-02/28/84, Contract F33615-83-C-1104, DTIC No. AD-B094-271

IV.10 Honeywell VHSIC Phase 2 Interim Technical Report #1, 11/01/84-03/31/-85, Contract F33615-84-C-1500

IV.11 Honeywell VHSIC Phase 2 Interim Technical Report #2, 04/01/85-09/30/-85, Contract F33615-84-C-1500

IV.12 IBM VHSIC Phase 2 Interim Technical Report #2, 02/16/85-08/09/85, Contract DAAK20-85-C-0376

IV.13 IBM VHSIC Phase 2 Interim Technical Report #3, 08/10/85-02/07/86, Contract DAAK20-85-C-0776

IV.14 TRW VHSIC Phase 2 Interim Technical Report #1, 11/01/84-05/31/85, Contract N00039-85-C-0111

IV.15 VHSIC Electrical Interface Specifications, Version 1.3, 03/20/86, For availability, contact J.P.Letellier, Code 5305, Naval Research Laboratory, Washington , DC.

IV.16 VHSIC Parallel Interface (PI) Bus Specification, Version 2.1, 09/26/86. For availability, contact J.P.Letellier, Code 5305 Naval Research Laboratory, Washington, DC.

IV.17 VHSIC Test and Maintenance (TM) Bus Specification, Version 1.2, 08/31/86. For availability, contact J.P.Letellier, Code 5305, Naval Research Laboratory, Washington, DC.

IV.18 VHSIC Element Test and Maintenance (ETM) Bus Specification, Version 1.1, 08/31/86. For availability, contact J.P.Letellier, Code 5305, Naval Research Laboratory, Washington, DC.

Section V   Phase 3

V.1 Hughes/Perkin Elmer Electron Beam Lithographic Equipment (VHSIC Phase 1), Contract DAAK20-81-C-0384, Interim Technical Report #1, 5/1/81-10/31/81, Report DELET TR-81-0384-1, DTIC No. AD-B067-304

V.2 Hughes/Perkin Elmer Electron Beam Lithographic Equipment (VHSIC Phase 1), Contract DAAK20-81-C-0384, Interim Technical Report #2, 11/1/81-4/31/82, Report DELET TR-81-0384-2, DTIC No. AD-B067-307

V.3 Hughes/Perkin Elmer Electron Beam Lithographic Equipment (VHSIC Phase 1), Contract DAAK20-81-C-0384, Interim Technical Report #3, 5/1/82-10/31/82, Report DELET TR-81-0384-3, DTIC No. AD-B067-296

V.4   A Review of Radiation Test Results on Phase 1 VHSIC Devices, M. Si-
        mons, Research Triangle Institute, Contract DNA001-83-C-0012,
        DNA-TR-85-196, 06/07/85

V.5   Radiation Hardness of VHSIC Phase 1 Technologies, R.C.Zittle,
        M.Simons, H.L.Hughes, and D.G.Platterer, Proceedings of GOMAC-85
        (Government Microelectronics Conference 1985), Orlando, FL, November
        5-7, 1985

V.6   VHSIC Briefs (Summary of VHSIC Technology Support Program), May 1986,
        Palisades Institute for Research Services, Contract N00039-86-C-0238

V.7   Proceedings of 1985 VHSIC Packaging Workshop, Naval Surface Weapons
        Center, Silver spring, MD, June 5-6, 1985, Palisades Institute for
        Research Services, DAAK20-84-C-0387

V.8   IBM Phase 1 Chip Testability Evaluation, Research Triangle Institute
        (RTI), Contract N00039-80-C-0648, Report TRI/2086/00-05Q, September
        1984

V.9   TRW Phase 1 Chip Testability Evaluation, Research Triangle Institute
        (RTI), Contract N00039-80-C-0648, Report RTI/412U/2086/02-02F, May
        1985, DTIC No. AD-BO95-054

V.10   VHSIC Briefs (Phase 3 Projects), May 1983 Palisades Institute for
        Research Services, Contract N00039-80-C-0448, DTIC No. AD-B073-845

V.11   VHSIC Briefs (Phase 3 Projects), November 1984, Palisades Institute
        for Research Services

Section VI - Management

VI.1   VHSIC Advanced Hands-on Applications Workshop III. Presentation
        Graphics, Johns Hopkins University, Applied Physics Laboratory,
        Laurel, MD, October 29-30, 1986

VI.2   Proceedings of 1982 VHSIC Conference, National Bureau of Standards,
        Gaithersburg, MD, August 3-6, 1982, DTIC Nos. AD-B066-597, 598, 599,
        600, 601

VI.3   Proceedings of 1983 VHSIC Conference, National Bureau of Standards,
        Gaithersburg, MD, September 19-21, 1983, DTIC Nos. AD-B076-951, 952,
        953, 954, 955, 956

VI.4   Proceedings of 1984 VHSIC Conference, Naval Surface Weapons Center,
        Silver Spring, MD, December 5-7, 1984, DTIC No. AD-B088-800

VI.5   Proceedings of 1985 VHSIC Conference, Naval Surface Weapons Center,
        Silver Spring, MD, December 4-6, 1985, DTIC No. AD-B098-014

VI.6   Proceedings of 1986 VHSIC Conference, Johns Hopkins University, Apoplied Physics Laboratory, Laurel, MD, December 8-10, 1986

VI.7   Abstracts of VHSIC Signal Processing Seminar, Naval Postgraduate School, Monterey, CA, June 17-18, 1986, Palisades Institute for Research Services

VI.8   VHSIC Instruction Kit, undated. From VHSIC Applications Workshops for DoD personnel and qualified contractors.

VI.9   VHSIC System Designer's Textbook, Johns Hopkins University Applied Physics Laboratory, Laurel, MD, 1986

VI.10 Very High Speed Integrated Circuits (VHSIC) Technology in Defense Systems, Draft DoD Directive, 09/05/86

VI.11 VHSIC Program Security Classification Guide, DoD Instruction 5210.75

VI.12 VHSIC Technology Security Program, DoD Instruction 5230.26

VI.13 Proceedings of Navy VHSIC Users Symposium, Johns Hopkins University, Applied Physics Laboratory, Laurel, MD, April 26-27, 1983, Report JHU/APL/SR-83-2, Contract N00024-83-C-5301, DTIC No. AD-C032-934

APPENDIX II

VHSIC CONTRACTORS AND KEY PERSONNEL

	PROGRAM MANAGER(S)	PHONE NO.
DoD VHSIC PROGRAM OFFICES		
DoD	E.D. Maynard, Jr.	202-697-4198
	LTC W.H.Freestone, Jr.	202-697-4198
	Lt Col H.R.Brown, III	202-697-4198
	D. Hayman	202-697-4198
Army	C.G. Thornton	201-544-2541
	H. Borkan	201-544-3241
Navy	LCDR P. Gariano, Jr.	202-692-6417
	LCDR H. Beasley	202-692-6417
Air Force	W.J. Edwards	513-255-2911
	J.M. Blasingame	513-255-3503
PHASE 1/ YIELD ENHANCEMENT		
Honeywell - Solid State Electronics Division	D. Burns	612-541-2066
Contract F33615-81-C-1527	D. Gunderson	612-541-2040
	R. Julkowski	612-541-2402
Hughes Aircraft - Industrial Electronic Group	R. Stone	619-931-5182
Contract DAAK20-81-C-0383	E. Gould	619-931-7092
IBM - Federal Systems Division	R. Estrada	703-367-4279
Contract N00039-81-C-0416	T. Mahar	703-367-5548
Texas Instruments - Equipment Group	J. Wilson	214-995-2395
Contract DAAK20-81-C-0382	D. Best	214-480-1321

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Contractor	Program Manager	Telephone
TRW - Military Electronics Division Motorola Contract N00039-81-C-0414	T. Zimmerman E. Daniels	213-535-3375 602-962-3094
Westinghouse - Advanced Technology Lab. National Semiconductor Contract F33615-81-C-1532	D. Sartorio J. Streb	301-765-6744 408-721-5448

PHASE 2

Honeywell - Solid State Electronics Division Contract F33615-84-C-1500	D. Burns G. Anderson D. Nielsen	612-541-2066 612-541-2045 612-541-2482
IBM - Federal System Division Contract DAAK20-85-C-0376	R. Estrada P. Johnson	703-367-4279 703-367-5547
TRW - Military Electronics Division Motorola Contract N00039-85-C-0111	T. Zimmerman L. D. Sikes	213-535-3375 602-244-4910

PHASE 3 - IDAS

Gould Defense Systems VHDL Design Workbench Contract DAAL01-85-C-0435	S. Swamy	312-640-4466
Sperry VHDL/MIXSIM Simulator Contract DAAL01-85-C-0436	L. Anderson	612-456-3871

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Contractor	Program Manager	Telephone
Intermetrics VHSIC Hardware Description Language (VHDL) Contract F33615-83-C-1003	V. Berman	301-657-3775
JRS Research Labs VHSIC/IDAS Microcode Compiler Demonstration Contract F33615-84-C-1422	E. Warshawsky	714-974-2201
United Technologies Microelectronic Center VHDL Independent Validation And Verification Contract F33615-85-C-1760	J. Costentino	303-594-8237
Honeywell Computer Science Lab Processor Synthesis Tool For VHDL Contract F33615-85-C-1261	S. Krolikosky	612-887-5701
General Electric Research Center VHDL Designer's Workstation Contract F33615-85-C-1862	J. Sturman	518-387-5457
Research Triangle Institute VHSIC Silicon Compiler Contract F33615-85-C-1863	J. Clary D. Franke	919-541-6951
National Semiconductor Corp Interface Between CMOS Process And Silicon Compiler Contract F33615-85-C-1867	J. Streb	408-721-5448
CAD Language Systems, Inc. Support To IEEE VHDL Standardization Contract F33615-86-C-1050	M. Shahdad	301-424-9445
Bell Northern Research Joint US/Canadian VHDL Rehost U.S. Participation Contract TBD	D. Agnew	613-726-4615

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Contractor	Program Manager	Telephone
Johns Hopkins U./APL VHDL Integration Contract N00024-85-C-5301	R. Siegel	301-953-5000 X4342
Research Triangle Institute ADAS Integration Contract N00039-86-R-0057	J. Clary	919-541-6951
Stanford Center For Integrated Systems Annotation Language for VHDL Contract F33615-86-C-1137	D. Luckham	415-723-1242
JRS Research Laboratories Advanced Ada Synthesis Tool Contract TBD	E. Warshawsky	714-974-2201
U. Of Southern California Advanced Component Design Using VHDL Contract TBD	A. Parker	213-743-5560
Research Triangle Institute/ U. Virginia Hierarchical Design For Testability Contract DAAL01-86-C-0039	J. Clary	919-541-6951
Dartmouth University Analog Design With VHDL Contract TBD	C. Hutchinson	603-646-2238
Rensselaer Polytechnic Institute Object-Oriented Chip Design Using VHDL Contract TBD	E. Rodgers	518-783-8182
Research Triangle Institute/OCTY, Inc. Artificial Intelligence Interface To The ADAS System DAAL01-86-C-0040	N. Kanopoulos	919-541-7341

Contractor	Program Manager	Telephone
PHASE 3 - LITHOGRAPHY		
Perkin Elmer X-Ray Lithography Equipment Contract DAAK20-84-4-0378	G. Ferrera	203-834-6610
GCA Advanced Wafer Imaging System Contract DAAL01-85-C-0460	P. Bachman	617-975-0000
PHASE 3 - RADIATION HARDENING		
Motorola Radiation Hardened Bulk CMOS Contract DNA001-84-C-0403	LCDR L. Cohn Defense Nuclear Agency (DNA)	202-325-7016
RCA Radiation Hardened CMOS/SOS Contract DNA001-84-C-0404	J.M. McGarrity Harry Diamond Lab (HDL)	202-394-3180
Westinghouse/National Semiconductor Radiation Hardened Bulk CMOS Contract DNA001-86-C-0134	LCDR L. Cohn DNA	202-325-7016
Hughes Aircraft Radiation Hardened CMOS/SOS Contract DNA001-84-C-0407	LCDR L. Cohn DNA	202-325-7016
Texas Instruments Radiation Hardened STL Bipolar Contract DNA001-86-C-0175	LCDR L. Cohn DNA	202-325-7016
TRW Radiation Hardened 3D Bipolar Contract DNA001-86-C-0186	LCDR L. Cohn DNA	202-325-7016

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Contractor	Program Manager	Telephone
Booz-Allen Electromagnetic Effects Chip Hardening Contract DAAL02-86-C-0042	R. Garver HDL	202-394-1403

PHASE 3 - OTHER CURRENT PROJECTS

Materials and Processes

Contractor	Program Manager	Telephone
Westinghouse VHSIC Silicon Starting Materials Contract N00039-83-C-0724	R.N. Thomas T.I. Braggins	412-256-1871
Hughes Research Laboratory Silicon Starting Materials For VHSIC Contract N00039-83-C-0725	R.C. Henderson P.K. Vasvdev	213-317-5000
Lawrence Livermore Laboratory Laser Pantography Natl. Lab. Task Assignment	L. Wood B. McWilliams	415-422-7286

Chip Packaging And Technology

Contractor	Program Manager	Telephone
Hughes Aircraft High Density Multilayer Packaging Devlopment Contract DAAK20-83-C-0429	R.P. Himmel R.I. Brown	714-759-2893 714-759-2497
Honeywell High Density Multilayer Packaging Development Contract DAAK20-83-C-0430	D. Gunderson R. Speilberger	612-541-2040 612-541-2924
Martin Marietta High Density Multilayer Packaging Development Contract DAAK20-84-C-0427	J. Fennimore G. Plite	305-356-2086 305-356-7909

Contractor	Program Manager	Telephone
Vanzetti Non-Destructive Evaluation Of Metallurgical Tape Bonds Contract F30602-86-C-0049	E.Blackburn	315-330-4055
Sonoscan Non-Destructive Package Screening Contract F30602-86-C-0050	E.Blackburn	315-330-4055
Hughes Aircraft VHSIC Low Dielectric Constant Printed Wiring Boards Contract F33615-84-C-1415	R.W. Siebold S.L. Oldhaus	
Reliability/Test		
TRW VHSIC Device Qualification N00039-86-C-0305	W. Adelman	213-535-5668
Research Triangle Institute Signal Processor Architecture Performance Evaluation Tool Contract DAAK20-80-C-2075	J. Clary G. Gray	919-541-6951
Texas Instruments Reliability/Test Contract F30602-81-C-0032	K. Kwiat	315-330-2047
Harris Tester Independent Support Software System (TISSS) Contract F30602-84-C-0168	D.Lehtomen	305-242-5617
General Dynamics VHSIC Impact On System Reliability Contract F30602-85-C-0007	B.Dudley	315-330-2608

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Contractor	Program Manager	Telephone
Honeywell Maintenance Concepts For VHSIC Contract F30602-85-C-0091	D.Richards	315-330-3476
IITRI VHSIC/VHSIC-Like Reliability Prediction Modeling Contract F30602-86-C-0261	P.Manno	315-330-2047
Genrad Advanced High Speed Test System Contract F33615-84-C-5076	J. Ross	408-946-6960
Research Triangle Institute On-Chip Self-Test And Repair Concepts Contract N00039-80-C-0648	J.B. Clary J.W. Watterson	919-541-6951

Phase 3 - Prior Projects   (Completed prior to 1986)

1. Architectural Studies

Contractor	Contract No.	Subject	DTIC No.
Arizona State U.	N00039-80-C-0511	Signal Processing Algorithms On Chips	AD-B072-124
Boeing	F33615-80-C-1196	Storage/Logic Arrays	AD-B954-381L
Carnegie Mellon	N00039-80-C-0640	A Hierarchical Design Approach For VHSIC	AD-B071-076
Lockheed	N00019-80-C-0610	Study Of VHSIC Applications In Naval Patrol Aircraft	AD-8074-271/2
Naval Air Development Ctr	In-House	Generalized Computer System Simulator For VHSIC	
Research Triangle Institute	DAAK20-80-C-0275	Signal Processor Architecture Performance Evaluation Tool	AD-B102-719L

Contractor	Contract No.	Subject	DTIC No.
Sanders Associates	F33615-80-C-1192	Memory Processor Study	AD-B068-519
Stanford Resch Institute	F30602-80-C-0303	Fault Tolerant Architecture For VHSIC	AD-B065-4998
Stanford Resch Institute	N00039-80-C-0571	Assignment Algorithms For Control Of VHSIC Chips	AD-B067-642
Texas Instrum.	DAAK20-80-C-0276	Data Flow Architecture	AD-B071-864/5-7
TRW	F33615-80-C-1202	Software Architecture Study	AD-B067-869
Univ. of Southern Calif.	N00039-80-C-0641	Architectures For Radar Signal Processing	

2. Lithography

Contractor	Contract No.	Subject	DTIC No.
American Science and Engineering	N00019-80-C-0568	Concentrating Collimating Illumination For X-Ray Lithography	AD-B073-623
AVCO Research	F19628-80-C-0176	High Intensity Pulsed Plasma X-Ray Source	AD-B066-469L
EBC Corp.	N00019-80-C-0618	Ultra High Speed Submicron Direct Write E-Beam System	
Hewlett Packard	DAAK20-80-C-0264	Advanced Resist Materials And Processes	
Hughes Research	N00019-80-C-0616	Improved Resists For Electron-Beam Lithography	
Hughes Research	DAAK20-80-C-0262	E-Beam Lithography Componenets For DirectlyAD-B094-565L Writing VHSIC	
Naval Research Laboratory	IN-HOUSE	X-Ray And E-Beam Effects On MOS Devices	

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Contractor	Contract No.	Subject	DTIC No.
Perkin Elmer	DAAK20-80-C-0261	Extension Of X-Ray Lithography Technology	AD-B074-215
Stanford Resch Institute	F33615-80-C-1194	Intense Plasma X-Ray Source For Submicron Lithography	
TRW	DAAK20-80-C-0263	Electron Beam System Software	AD-B078-420/421
Varian Associates	F19628-80-C-0173	Develop Direct Write E-Beam Lithography Components	

3. Processing

Contractor	Contract No.	Subject	DTIC No.
AVCO Research	N00039-80-C-0589	Coronaphoresis For Gas Purification	AD-B077-419
Cornell Univ.	F33615-80-C-1197	Improved Crystal Quality Of Silicon On Insulated Substrates	
Hughes Research	N00019-80-C-0616	Low Temperature Silicon Epitaxy	
Hughes Research	DAAK20-80-C-0268	Low Temperature Photochemical Processing For VHSIC Applications	AD-B085-497L
Hughes Research	DAAK20-80-C-0269	Laser Annealing	
Hughes Research	DAAK20-80-C-0270	Electron Beam Processing	
Perkin Elmer	DAAK20-80-C-0265	Extend Microlithography Technology Through Plasma Etching	AD-B085-912

4. Design Automation

Contractor	Contract No.	Subject	DTIC No.
Cal Inst. Techn	N00014-79-C-0924	Demonstrate Use Of VLSI Design Rules, Standards, And Interfaces	AD-B077-602/3/4
GE	F33615-80-C-1083	CAD For Testable LSI	AD-B095-571L

Contractor	Contract No.	Subject	DTIC No.
Sandia Lab	P.O. 81-19638/39	Critical VHSIC Design Tools	AD-B067-139
TRW	F33615-80-C-1198	Transportability Of CAD Data	AD-B075-616
Univ Southern California	DAAK20-80-C-0278	Design Automation	

5. Material and Characterization

Contractor	Contract No.	Subject	DTIC No.
Cornell Univ.	F33615-80-C-1197	Analytical Methods For Detecting Substrate Defects	
Hughes Aircraft	DAAK20-80-C-0273	Refractory Metal For Interconnection	AD-B082-339
Texas Instr	N00039-83-C-0722	X-Ray Diagnostic Techniques For VHSIC Silicon	
VTI, Inc.	N00039-83-C-0723	VHSIC Starting Materials - Diagnostics	
Westinghouse	DAAK20-80-C-0271	Mobility/Drift Velocity Measurement In Inversion Layers	
Westinghouse	F33615-79-C-1946	Improved SOS For VHSIC	AD-B078-171
Westinghouse	N00039-80-C-0662	Low Defect Density Silicon Substrates For NMOS	AD-B102-419L

6. Device Technology

Contractor	Contract No.	Subject	DTIC No.
Cornell Univ.	F33615-80-C-1197	Simple Submicron Device Models For Circuit Simulation	AD-B958-232L
Cornell Univ.	F33615-80-C-1197	Submicron Devices: Exact Simulation And Simple Models	
GE	DAAK20-80-C-0272	Development Of MESFET Silicon On Sapphire For IC Gates	AD-B068-304

Contractor	Contract No.	Subject	DTIC No.
Hughes Aircraft	N00019-80-C-0616	Static Induction Transistor (SIT) Logic Technology	
Rockwell	DAAK20-80-C-0274	Low Resistivity Gates For CMOS ICs	AD-B066-109L
The Analytical Science Corp.	N00039-80-C-0086	Industry Impact Of VHSIC Program: A Preliminary Analysis	
Westinghouse	F33615-80-C-1199	Electronically Alterable ROM For VHSIC	AD-B080-958

7. Packaging

Contractor	Contract No.	Subject	DTIC No.
GE	F33615-80-C-1191	Improved Package For VHSIC	AD-B080-965
Honeywell	DAAK20-80-C-0267	Electronic Packaging For VHSIC	AD-B070-866
Raytheon	F33615-80-C-1193	High Density, High Performance Hybrid Circuit Technology	AD-B069-485
Westinghouse	F33615-82-C-5047	HCC-Compatible PWB Materials	

8. Testing and Reliability

Contractor	Contract No.	Subject	DTIC No.
Hughes Aircraft	DAAK20-80-C-0277	Failure Management Design System	AD-B074-223
Hughes Aircraft	F30602-80-C-0321	Electron Beam Circuit Tester	AD-B073-808
Hughes Aircraft	N00039-80-C-0625	Acoustic Microscopy For Inspection Of VHSIC Chips	
University of Illinois	N00039-80-C-0556	Reliable, High Performance VHSIC System	AD-B089-167
National Bureau Of Standards	N00019-79-IP-990003	Measurement Technology For VHSIC	

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Contractor	Contract No.	Subject	DTIC No.
Prospective Computer Analysts	F30602-84-C-0167	Tester Independent Support Software System	AD-B087-155
Research Triangle Institute	NU0039-80-C-0648	Identify And Assess On-Chip Self Test And Repair Concepts	
Rockwell	F33615-82-C-5110	Test Structure Development	
Stanford Univ.	DAAK20-80-C-0266	Testing VHSIC Devices	
Texas Instrum.	F30602-81-C-0032	Develop Test Technology For VHSIC	
University of Southern Cal.	N00039-80-C-0641	Design For Testability And Reliability	AD-B086-080
Aerospace/JPL	F4071-83-C-0084	VHSIC Yield Enhancement Test Structure	

APPENDIX III

LIST OF EXHIBITORS - 1986 ANNUAL VHSIC CONFERENCE

AT&T
Guilford Center
Greensboro, NC 27420
Michael Golden, 919-279-4192

Control Data/ VTC Corp.
Rockville, MD 20852
Richard Balestra, 301-468-8183

General Electric
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Syracuse, NY 13221
John May, 315-456-2412

Harris Semiconductor
Government Systems Division
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Lee Allain, 305-729-5270

Honeywell
Systems and Research Center
Minneapolis, MN 55418
Murray Cooper, 612-782-7389

Hughes Aircraft
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Robert Stone, 619-931-5182

IBM
Federal Systems Division
Manassas, VA 22110
Jay Harford, 703-367-1041

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Carolyn Elson, 617-661-1840

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MICARL
Mesa, AZ 85202
Ed Daniels, 602-962-3094

National Semiconductor
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Jerry Streb, 408-721-5448

Performance Semiconductor
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Les Wellborn, 408-734-8200

Perkin Elmer
EVT Division
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Moorestown, NJ 08057
Fred Jones, 609-866-6453

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Linus Cordes, 617-470-9050

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Research Triangle Park, NC 27709
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Dallas, TX 75266
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Electronics & Defense Division
Redondo Beach, CA 90278
Tom Zimmerman, 213-536-2251

Westinghouse
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Mike Lucas, 301-765-5037

APPENDIX IV

STATEMENT OF WORK   -   PHASE 1

INTRODUCTION

The purpose of the VHSIC program is, to meet presently defined and future military system needs while providing an increased ability, on the part of the U.S. electronics industry, to respond fully, quickly, and cost effectively to the DoD's continuing and rapidly expanding requirements for complex, high speed signal processing functions in its electronic subsystems and systems. The program is divided into four parts called Phase 0, 1, 2, and 3, each with distinct and important goals.

The end goal of the entire program is to reach a capability for advanced systems performance based on availability of ICs with submicrometer feature sizes. Phases 0, 1, and 2 are being carried out consecutively, while Phase 3 is being carried out concurrently with Phases 0, 1, and 2.

A glossary of VHSIC terms and acronyms is included in Section C.5.

SCOPE

Based on analyses and/or investigations of the tasks described in the Statement of Work for the Program Definition Phase (Phase 0), efforts in Phase 1 shall be directed into two broad areas conducted concurrently over a period of 36 months or less:

Phase 1a shall provide for the development of 1.25 micrometer technology in terms of process development, DAST, VHSIC circuit design, pilot fabrication, and subsystem brassboard development and evaluation. A sufficient number of types of 1.25 micrometer VHSIC chips, meeting the minimum goals of 25 MHz on-chip clock rate and 5×10^{11} gate $-$ Hz/cm^2 Functional Throughput Rate (FTR), will be developed in order to provide adequate evaluation and effective systems demonstrations of VHSIC subsystem brassboards. Consideration shall be given to the extendability of the 1.25 micrometer technology to 0.5 micrometer VHSIC circuits.

Phase 1b goals are to provide for the development of a 0.5 micrometer VHSIC technology and the fabrication of test chips which demonstrate that the design and fabrication of VHSIC chips on a pilot production basis will be feasible during Phase 2. In attempting to meet 0.5 micrometer goals, all critical problems will be identified and specific methods of approach for their solution will be addressed. The processing, DAST, and other technology developments needed in order to meet the VHSIC end goals of 10^{13} gate-Hz/cm^2 FTR at a minimum on chip clock rate of 100 MHz will be accomplished in Phase 1b.

Phase 3 Transfer of Technology - In each of Phases 1a and 1b, maximum use shall be made of the technologies being developed under

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Phase 3 of the overall VHSIC program. Development of an E-beam lithographic machine to be made available for purchase and use in Phase 2 may be accomplished as an alternate task in Phase 1b.

Tradeoffs for Reliability – It is one of the major intents of the VHSIC program to achieve higher reliability and greater testability of chips and chip sets in DoD applications than is currently available. This goal is considered important enough to allow chip area and functional throughput trade-offs to be made in order to gain the space and functional capacity for effective self-test operations.

REQUIREMENTS FOR PHASE 1a [1.25 MICROMETER]

Chip Technology and Fabrication

Chip technology and processing techniques shall be developed to implement VHSIC circuits with 1.25 micrometer features. Emphasis shall be given to factors which affect the usefulness of the technology for military applications. These factors include power supply requirements, noise immunity, chip interface standardization, nuclear radiation tolerance, reliable operation in a military environment, and availability from more than one source. A compatible set of processing steps shall be developed which will provide acceptable yield meeting VHSIC goals of high device density, high level of integration, and high operating speed. Processing steps such as initial wafer preparation, defect analysis, lithography, oxidation, patterning, doping, annealing, metalization and passivation should be included.

Chip manufacturing techniques shall be developed to fabricate VHSIC circuits using the processing techniques developed under C.3.1.1. The manufacturing techniques development shall include computer aided manufacturing, process control, and the equipment refinements necessary to realize cost-effective and consistent yields for VHSIC circuits in a pilot production line environment. Typical device parameters and their variations, detailed test and measurement techniques, process control parameters, ranges, and tolerance shall be established, documented and demonstrated.

A pilot production line with sufficient automation to achieve the contractor's projected requirements for VHSIC chips shall be established, documented, and demonstrated. A plan to satisfy DoD production requirements as projected by the contractor shall be documented. Evaluation chips shall be fabricated, tested, and delivered to validate the control and repeatability of performance parameters, chip yield and wafer throughput. A cost model of the pilot line shall be formulated to establish the acquisition costs for VHSIC chips.

Packages for the VHSIC circuits to ensure the realization of the reliability requirements of section C.3.1.5 shall be designed, developed, fabricated, tested, and delivered. The packaging approach shall provide solutions to the problems of hermeticity and moisture content, thermal management, operating speed, interconnections, interfaces, assembly, standardization, solderability, mechanical strength, and soft errors due to nuclear particle effects.

Trade-offs among the following environmental and reliability requirements/goals, fabrication complexity and cost, and chip performance shall be analyzed in order to permit assessment of the difficulty of achieving these requirements/goals for packaged VHSIC chips.

Operate as a goal over the case temperature range of -55°C to $+125^\circ$C.

Operate without radiation induced failures in a radiation environment of at least 10^4 rads [Si], with a goal of 5×10^4 rads [Si].

Operate without radiation induced permanent failures after a transient radiation dose of at least 10^8 rads [Si]/s, with a goal of 10^9 rads [Si]/s for a 10 nanosecond radiation pulse.

Operate without transient upset through a radiation pulse of 10^7 rads [Si]/s for a 10 nanosecond radiation pulse.

Operate without permanent damage after neutron radiation dose of at least 10^{11} neutrons/cm^2, 1 MeV equivalent.

As an end goal with a mature process, have failure rates, after screening and burn-in, not exceeding .006% per 1000 hours at 60% confidence level both while operating and while stored over the range -55°C to $+85^\circ$C case temperature.

DAST [Design, Architecture, Software, Test]

An architectural approach and hierarchical chip design methodology for use with computer aided design facilities shall be developed and documented to provide VHSIC circuits suitable for broad DoD systems applications. New and/or improved design and architectural concepts, standard interfaces and conventions shall be developed to minimize the number of custom circuits for signal processing applications in addition to reducing the costs of whatever remaining customization is necessary for particular applications. Approaches which minimize the use of peripheral SSI and MSI components and which provide for realization of this circuitry for specific applications using low cost LSI/VLSI circuits shall be included. Develop and document a description of the VHSIC chips and their

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interfaces. Provide detailed definitions of chip primitives,
functional processing modules, macrocells or similar partitions
which are used in the design processes.

Support systems such as higher order language software development
systems which facilitate the cost effective programming and use of
VHSICs in DoD systems shall be developed. Interfaces between chip
descriptions in HDL, CAD software used to design the chip, and user
programming software shall be developed. An HOL shall be used for
programming user programmable VHSIC chips. Ada shall be used as the
HOL unless otherwise justified by the contractor and approved by the
contracting officer. Off-chip compilers may be used as appropriate.

Computer Aided Design [CAD] software, aids, and techniques shall be
developed with the flexibility to cover a broad range of military
signal and data processing problems including very high performance
and/or low cost applications. Design costs and design time shall be
estimated for various levels of circuit complexity. A common artwork
description language shall be established for transfer of patterns
from design groups to fabrication areas. A common test language
shall also be established for transfer of test pattern sets from
test generators to fabrication testing facilities and shall be based
on the DoD ATLAS test language unless an alternate is approved
through the PCO. A higher level hardware description language shall
be established for transfer of data among CAD, computer aided
manufacturing [CAM], and computer aided testing [CAT].
Recommendations for appropriate DoD standards to be developed from
these languages shall be submitted. CAD tools shall be defined to
support the entire design process including definition, design,
implementation, functional verification, chip and subsystem physical
design, physical verification, and testing and design for
testability and reliability. CAD tools shall be integrated with a
unitized data base into which data items need be entered only once
and are then available to all tools and aids within the CAD system.

Simulation techniques to validate subsystem chip designs shall be
established compatible with the speed, complexity, and design
parameters of VHSIC circuits and subsystems with clearly defined
interfaces between simulation levels. The simulation techniques
will include the models, model parameters, process and device
characteristics, data and computational algorithms which are
required for cost-effective simulation of the fabrication process,
device, circuit, gate, logic, register transfer, and subsystem
functional levels. The simulation techniques shall be capable of
modeling the operation of brassboard subsystems containing several
VHSIC chips.

Design techniques shall be developed, documented, and demonstrated
which provide increased reliability and testability of chip
performance through the inclusion of on-chip testing and fault

tolerant designs. Design techniques shall be developed, documented, and demonstrated which minimize electromagnetic interference.

VHSIC Chip and Subsystem Development

For each of the specific military subsystems which were proposed by the contractor and selected by the government (prior to contract award) for brassboard demonstration, the contractor shall perform the followng tasks:

Refine the system analysis to further define the subsystem architecture, design, and software requirements. This analysis shall include life cycle cost modeling, hardware/software trade-offs, functional commonality, I/O requirements, HOL (Ada) software requirements, memory requirements and functional throughput requirements, and shall result in detailed functional, hardware, and software specifications. The design and performance trade-offs among subsystem architectures, software, algorithms, fault tolerance and functional modules shall be determined and documented.

Using the analysis and subsystem specification developed in C.3.3.1, develop and document detailed functional definitions of subsystem software, algorithms, functional processing modules and VHSIC chips. In defining VHSIC chips, emphasis shall be placed on minimizing the use of SSI and MSI components and on achieving cnip-set/macrocell flexioility, commonality, and testaoility. The detailed functional definitions for each chip shall be subject to review and approval within 2 weeks by the contracting officer prior to starting task C.3.3.3 for that cnip.

Design, fabricate, package, test and document the VHSIC chips required to implement the specific suosystem defined under C.3.3.1. Chip design/architecture shall include design for testablity as well as the functional requirements developed in C.3.3.2. Cnip documentation shall include complete functional, electrical, programming, and testing specifications, a high level hardware description language description, and an application guide. Tests shall include electrical characterization over the specified temperature range and functional testing which demonstrates the efficiency of the design for testability. Environmental and reliability testing and failure analysis shall be performed to provide an indication that packaged VHSIC chips can satisfy the requirements/goals of C.3.1.5.

Design, develop, assemble, functionally program, test and document a brassboard of the subsystem defined in C.3.3.1.

Demonstrate and document the performance and test results and

deliver the subsystem brassboard containing VHSIC chips which are operable as the signal/data processing portions of the specific military subsystem selected by the government. This demonstration may be conducted under self-contained laboratory conditions with input data representative of the system environment. Develop and deliver a test plan for conducting a comprehensive system demonstration subsequent to the completion of Phase 1 which will include environmental and electromagnetic vulnerability assessments.

VHSIC Technology Transfer

A viable and effective procedure for making VHSIC chips available for sale to all other DoD contractors and government laboratories in a timely and affordable manner shall be developed. At least two approaches shall be considered: [1] providing a processing service alone, and [2] providing both processing and design/architecture services. The interfaces and input requirements for each approach shall be clearly defined. A second source procedure based on using the same chip specifications and the same chip functional performance for all sources shall be developed. This procedure shall include the schedule for availability and the restrictions placed on the second source.

Establish a viable and effective procedure for making equipment and software developed under this program available as early as possible for use by DoD contractors and government laboratories, preferably as completely engineered equipment and fully documented software with full operating descriptions.

Establish a viable and effective procedure for the insertion of VHSIC chips and technology into any appropriate existing and developing DoD equipments. Identify candidate systems and describe performance enhancements and cost benefits that can be achieved through VHSIC Technology Insertion efforts.

REQUIREMENTS FOR PHASE 1b [0.5 MICROMETER]

Chip Technology and Fabrication

Chip technology and processing techniques shall be developed to establish the feasibility of implementing VHSIC circuits with 0.5 micrometer features. In developing chip technology, trade-off studies shall be performed to determine the difficulty of developing the 0.5 micrometer technology and the extendability of the technology developed under C.3.1.1. The feasibility of the technology for military applications shall be assessed using the factors and processing steps listed in C.3.1.1. Determine the limitations and capabilities of the selected 0.5 micrometer technologies. Test chips and/or circuits shall be fabricated and evaluated to demonstrate the feasibility. A simple cost model shall

be developed in order to estimate the projected production costs of 0.5 micrometer VHSIC chips.

Determine and evaluate the packaging requirements for VHSIC circuits which will operate in accordance with military conditions specified in Section C.3.1.5.

Based on the efforts performed in Sections C.4.1.1 and C.4.1.2 prepare a development plan for the design and fabrication of VHSIC chips meeting the goals of Section C.2.2.

Requirements shall be determined and plans prepared for development of key equipment needed during the overall course of the program to achieve 0.5 micrometer VHSIC circuits. This includes equipment such as dry plasma etchers, automatic testers, design simulators, lithographic machines, etc. Among other aspects, factors to be addressed include the use of such equipment in fabrication/manufacturing and development of needed input data, format, and language.

[FOR ALTERNATE PROPOSAL] Electron Beam Lithographic (EBL) equipment necessary to fabricate 0.5 micrometer feature size VHSIC chips on a pilot line basis shall be developed. Equipment developed in this alternate task shall be made available for commerical sale to DoD contractors. At the option of the government the Phase 2 VHSIC contractors will be afforded equal priority first rights of refusal on the first machines of each type offered for sale. In performing the following subtasks, specified parameters, where applicable, shall be measured to 2 sigma error limits at a 95% confidence level unless otherwise noted and will apply over the entire writing area.

System Definition - The EBL system shall consist of, but not be limited to, an electro-optical column, work chamber, stage, vacuum system, system software, pattern generator, automated loading system, and a computer aided design interface to be compatible with the artwork descriptive language developed in C.3.2.3 and C.4.2.3. The contractor shall select, configure, and evaluate an electron optical column consisting of an electron gun, lenses, beam blanking, beam forming, and deflection systems capable of producing a low distortion focused electron beam scanned at high speeds. The electron column shall be compatible with EBL system performance and throughput requirements. The electron source lifetime snall be compatible with an EBL system uptime of 90% on a yearly basis, and the emission stability, both DC and broadband, of the electron gun over the life of the source shall be +1.0%. The stage will handle and permit exposure over the entire surface of both square glass plates and round semiconductor wafers having dimensions up to 160 mm X 160 mm with appropriate thickness and flatness. A pattern generator must be provided with at least a minimum set of design shapes including rectangles, trapezoids, and parallelograms (disc

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would also be preferred); these shapes will be used to fabricate the features used in exposing an IC level. The speed of the pattern generator shall be such that it poses no limitations on throughput required by C.4.1.5.3.

System Performance - Design, develop, fabricate, evaluate, and document an EBL system suitable for pattern writing in 0.5 um PMMA resist on 1000 Å of silicon dioxide on a silicon substrate demonstrating: [1] a resolution of 0.5 um half pitch lines and spaces; [2] a roughness of one edge of a 0.5 um linewidth of less than 0.05 um over a writing field; [3] a butting error of all lines meeting at scan field boundaries of +0.1 um or less; [4] a base address structure of 0.05 um or less and variable to accommodate different applications; [5] an overlay precision of +0.1 um or better; and [o] control of proximity effects through the use of integral software and/or hardware to calculate the correct exposure and/or shapes and to provide exposure compensation and/or shaping as a function of geometry to maintain dimensional accuracy to within +0.05 um. The above patterns will be etched in the silicon dioxide and the resultant geometries measured to demonstrate the above resolution, overlay and butting accuracy specifications, and proximity effects; the thicknesses of resist and oxide will be compatible with the process fabrication of 0.5 um feature size devices.

System Throughput - Optimize the EBL system to achieve the following minimum requirements of: An overall throughput consisting of at least four [4]-4" diameter wafer levels per hour or more through a direct write E-beam exposure of a positive resist having a sensitivity of 2×10^{-5} coulomb/cm^2 or less while maintaining at least 95% of its initial thickness through resist development. The overall throughput will be demonstrated with a selected test pattern containing 10^6 geometries/cm^2 and featuring the following distribution of minimum geometries over 30% of the 4" diameter wafer area:

  [1] 5% of total patterned area at 0.5 um resolution [1/2 pitch].
  [2] 10% of total patterned area at 1 um resolution.
  [3] 15% of total patterned area at 2 um resolution.
The machine performance shall not be limited by the electron optics writing speed even for resists as sensitive as 5×10^{-7} coulomb/cm^2.

System Environment, Reliability, and Acceptance Test - The system environment shall be consistent with class 100 type clean room facilities. The reliability of the system should be capable of 90% uptime with around the clock operation, seven [7] days per week for fifty-two [52] weeks including scheduled maintenance not to exceed 4 hours per week. The contractor shall develop and submit for approval a suitable set of patterns and tests to demonstrate compliance with the listed specifications of C.4.1.5.2 and C.4.1.5.3. The acceptance test will be accomplished initially at the

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equipment development site and finally upon installation at the contractor's pilot line facility.

DAST [Design, Architecture, Software, Test]

DAST developments conducted in Phase 1a in accordance with Section C.3.2 shall be reviewed, analyzed, and documented with regard to their effective use for 0.5 micrometer VHSIC circuits. Further development shall be performed and documented in order to establish the requirements and tools appropriate for realizing submicrometer speed, gate density, and functional complexity capabilities.

Update the Architectural Approach and Chip Design Methodology developed in C.3.2.1.

Update the Chip Support Software approach developed in C.3.2.2

Update the Computer Aided Design approach developed in C.3.2.3.

Update the Simulation Techniques developed in C.3.2.4.

Update the VHSIC Testability and Electromagnetic Vulnerability approach developed in C.3.2.5.

System Application

VHSIC circuit and subsystem developments conducted in Phase 1a shall be reviewed and analyzed with regard to their use of the 0.5 micrometer technology developed under sections C.4.1 and C.4.2. Preliminary functional and design definition of VHSIC chips and chip sets shall be performed to establish the feasibility of meeting the broad objectives of the VHSIC program as described in Sections C.1 and C.2. Determine the impact of the 0.5 micrometer technology on system performance and mission capability for at least one system of interest to each service.

VHSIC Technology Transfer

Documentation of procedures prepared under C.3.4 for 1.25 micrometer VHSIC circuits shall be reviewed by the contractor and modifications recommended for making 0.5 micrometer VHSIC chips, technology, software, and equipment available to DoD contractors and laboratories.

GLOSSARY

VHSIC - Acronym for Very High Speed Integrated Circuits. This acronym was developed to describe the program to develop very large scale integrated circuits applicable to DoD needs, particularly very high speed signal processing. The speed-density product

figure-of-merit goal is 10^{13} gate-Hz/cm . The acronym is also used to describe the integrated circuits that will be developed under the program.

Phase 0 - Refers to the program part called "Program Definition" to provide a pl n and approach for Phase 1 and Phase 2.

Phase 1 - Refers to the parts of the program during which electronic brassboard subsystems are constructed by about 1984 using VHSICs based on 1.25 micrometer minimum feature sizes [Phase 1a], and in which development work is carried out to achieve VHSICs based on submicrometer feaure sizes [Phase 1b].

Phase 2 - Refers to the program part oriented to: (1) the system demonstration of the electronic brassboard subsystems, and (2) the achievement of VHSICs with submicrometer [nominally 0.5] feature sizes by about 1986.

Phase 3 - Technology efforts which are generic in nature and which are supportive of Phase 1 and Phase 2.

VHSIC Architecture - A structure by which VHSIC devices are interconnected, addressed and programmed to meet design objectives of application algorithms. This definition includes interconnection or bussing, instruction set, special functions, control, addressing I/O schemes made compatible with one operating system including executive and language programming issues. Interconnection of VHSIC devices will produce a machine which can be used to perform many signal processing as well as generic logic and arithmetic functions.

Subsystem - This refers to an assembly of ICs and related components such as a signal/data processor that performs a function which can be incorporated into an entire system such as an aircraft, missile or communication system.

System Demonstration - This refers to the validation and testing of an electronic subsystem in a system test bed.

Subsystem Brassboard - An operating assembly for evaluation purposes with proper input and output terminals, containing ICs and other components [as required] all assembled, interconnected and packaged. It is differentiated from both a laboratory assembly [breadboard] and a fully engineered production prototype.

DAST - Acronym for Design, Architecture, Software, and Test.

FTR - Functional Throughput Rate is the product of on chip clocking speed (reciprocal of 4 gate delays) in Hertz and the gate density in gates per square cm .

Chip - A single monolithic silicon integrated circuit.

Automated Pilot Line - A facility consistng of equipment and personnel which is capaole of faoricating, packaging, and testing VHSIC chips on a sustained basis. It employs CAM tecnniques and automatic controls necessary to assure repeatability and consistent yield. It need not be dedicated only to VHSIC chips.

CAD - Computer Aided Design

CAM - Computer Aided Manufacture. Within the context of the VHSIC Program, CAM is defined to mean tne inclusion of sufficient automatic processing controls and automatic data collection to assure that the fabrication parameters are-reproducible within predictable limits.

CAT - Computer Aided Testing

HOL - Higher Order Language

HDL - Higner Description Language. Within tne context of VHSIC, this HDL is defined as that language which defines a chip functionally, physically, structurally and in terms of environmental restrictions and timing restraints. It would essentially replace the data sheet in providing a computer readable data file for transfer of information about a chip or subsystem design between CAD systems.

EBL - Electron Beam Lithographic (machine)

APPENDIX V

STATEMENT OF WORK   -   PHASE 2

VERY HIGH SPEED INTEGRATED CIRCUITS (VHSIC)

PHASE 2 SUBMICROMETER TECHNOLOGY DEVELOPMENT

1.0 INTRODUCTION

The purpose of the Very High Speed Integrated Circuits (VHSIC) program
is to meet presently defined and future military system needs while
providing an increased ability, on the part of the U.S. electronics
industry, to respond fully and quickly to the DoD's continuing and rapidly
expanding requirements for complex, high-speed, signal-processing functions
in its electronic subsystems and systems. The overall VHSIC program,
initiated in 1979, was divided into four parts: called Phases 0,1,2 and
3. Phase 0 was the program definition effort for Phase 1. Phase 1 was
initiated in May 1981 to develop signal processing chips and brassboards
based on 1.25 micrometer technologies and now includes chip testing, chip
qualification, and chip cost reduction through a comprehensive yield
enhancement program. Phase 2 now encompasses: (1) Phase 1 technology
insertion, (2) Integrated Design Automation System (IDAS), and (3)
submicrometer technology. The Phase 1 technology insertion effort provides
for brassboard development, testing, and evaluation through field testing.
The IDAS program is the development of a comprehensive system-level
computer-aided design system and the definition and implementation of a
VHSIC Hardware Description Language (VHDL). Phase 3 consists of related
support technology development and study efforts.

This Statement of Work (SOW) covers only the Phase 2 Submicrometer
Technology Development portion of the VHSIC program. The objective of the
VHSIC Submicrometer Technology Development program is major weapon system
performance improvement provided by halfmicrometer IC fabrication
technologies. While emphasis is placed on signal processing, data
processing applications are not excluded. Innovative architectures and
approaches are required.

2.0 SCOPE

The scope of this program encompasses six areas of advanced development
work: (1) baseline process technology, (2) packaging, (3) design, (4)
applications, (5) technology transfer, and (6) enhanced process technology.
A sufficient number of types of halfmicrometer VHSIC chips meeting the
minimum requirements of 100 MHz on-chip clock rate and 1×10^{13}
gate-Hz/cm^2 Functional Throughput Rate (FTR), will be developed in order
to provide adequate evaluation of, and effective systems demonstrations of
VHSIC subsystem brassboards. "Process technology" requires process
development, materials, lithography and resists, modeling, scaling and
simulation, process test chips, defect analysis, subfunctional test
vehicles, VHSIC chip fabrication, testing, manufacturing techniques and
pilot line. "Packaging" requires tracking present R&D and manufacturing
technology efforts for chip packages and printed circuit boards, and
development of multi-chip and second-level packages for boards and modules.

"Design" requires integration of VHDL and IDAS tools, development of a design methodology to include testability and fault tolerance, VHSIC chip design and layout, and development of VHDL descriptions and chip simulation. "Applications" requires analysis of military weapon system requirements in the 1990's, leading to a system architecture and the definition of a set of specifically designed VHSIC chips which shall satisfy the broadest feasible range of these requirements, a brassboard module demonstration, software development plus one or more optional major brassboard demonstrations for halfmicrometer technology insertion into an actual weapon system. "Technology transfer" requires development of interoperability standards, chip availability planning, a second-source process transfer plan and an external foundry service design demonstration.

A tradeoff radiation environment, section 4.2, requires processing and design approaches early in the program in anticipation of future applications. The selected process shall, as a minimum, support one of the two environments called out in section 4.2.

Environmental, reliability and testability requirements are emphasized in this program. The full potential capability and advantages of halfmicrometer technology is to be demonstrated in a working brassboard module supported by peripheral signal input, output, data processing and display equipment in a laboratory environment.

Phase 3 Transfer of Technology - In Phase 2 maximum use shall be made of the technologies being developed under Phase 3 of the overall VHSIC program.

Tradeoffs for Reliability - It is one of the major intents of the VHSIC program to achieve higher reliability and greater testability of chips and chip sets in DoD applications than is currently available. This goal is considered important enough to allow chip area and functional throughput trade-offs to be made in order to gain the space and functional capacity for effective self-test operations.

3.0 REQUIREMENTS

The Contractor shall provide all services, supplies and facilities necessary to accomplish the following:

3.1 Process Technology

The objective of this task is to develop a set of processing steps which shall provide acceptable yield meeting VHSIC goals of 100 MHz on-chip clock rate and 1×10^{13} Gate-Hz/cm^2 Functional Throughput Rate at halfmicrometer design rules. Emphasis shall be given to factors which affect the usefulness of the technology for military applications, such as the environmental, reliability and testability requirements listed in section 4.0.

3.1.1 Process Development

3.1.1.1 Baseline Process Development: A baseline process tolerant to the radiation environment listed in Section 4.2.1 shall be established, demonstrated by results from functional circuit

elements and documented. A multi-level (minimum of 2-interconnect layers) interconnect system is required. The metallization system shall be defined and design rules determined consistent with other reliability, performance and producibility requirements and commensurate with halfmicrometer minimum feature size. This aggressive metal pitch shall be sufficiently small to achieve the maximum performance benefits of the halfmicrometer process technology.

The contractor shall not begin fabrication of the intermediate test vehicle (See 3.1.6, 3.3.2 and 3.4.3) and functional VHSIC chips (See 3.1.7) until forty-five days after submission of the baseline process to the Government for approval or until receipt of Government approval to proceed, whichever comes first.

3.1.1.2 Enhanced Process Development: Processing steps and device configurations which enhance the tolerance to the radiation effects listed in section 4.2.2 shall be developed and implemented. In selecting processing alternatives, attention shall be given to the effects of radiative processes, high temperature treatments, etc. on radiation hardness and reliability. Structural variations such as alternate isolation and doping schemes should be considered. Where possible, the process and structure should be compatible with the baseline process and chip layout. Test chips and structures (section 3.1.5) shall be fabricated and tested. Special test structures may be required to fully evaluate the radiation effects. The contractor shall not begin fabrication of the intermediate test vehicle (See 3.1.6, 3.3.2 and 3.4.3) and functional VHSIC chips (See 3.1.7) until forty-five days after submission of the enhanced process to the Government for approval or until receipt of Government approval to proceed, whichever comes first.

3.1.2 Materials: Materials characteristics required to process and produce halfmicrometer structures, consistent with device performance and yield, shall be defined, specified, and documented. The bulk silicon wafers or epitaxial silicon starting material shall be thoroughly characterized, including electrical properties, chemical impurities and their concentrations, structural defects and density to determine the degree of conformance to the established materials characteristics. Other chemicals, gases, targets and materials used to process the silicon shall likewise be characterized such that the influence of material quality can be correlated with device performance on a wafer by wafer basis.

3.1.3 Lithography And Resists: A lithographic process to implement VHSIC chips with halfmicrometer minimum feature sizes shall be demonstrated and optimized for yield and cost effectiveness. The overall error budget for the lithography or directed beam approach used for device definition in all associated fabrication process steps that impact performance through the introduction of dimensional errors shall be calculated and documented. Yield as a function of error variance, chip size, and chip complexity shall be projected and documented. Machine to machine error, where duplicate machine installations are used, shall be included in any error budget calculations. Fabrication process throughput rates and throughput limiting fabrication machinery for various mixes of circuit details, yield as a function of design rules, circuit complexity and

chip size shall be determined. The lithographic process impacts on the costs of ownership and operation of a halfmicrometer production environment VHSIC process shall be estimated and documented. An automated system for generating geometrical patterns on silicon wafers shall be established. The input-data format and language shall be defined and documented, with particular attention given to compatibility with the computer-aided design tools used. High-resolution, high-sensitivity resists may be developed as necessary to optimize this process.

3.1.4 Modeling, Scaling And Simulation: The process and devices shall be modeled using appropriate simulation tools so that the effects of scaling to halfmicrometer minimum feature size can be determined prior to VHSIC chip design. These techniques shall be documented and used to optimize the process for yield, performance and cost effectiveness in producing devices with halfmicrometer feature size.

3.1.5 Process Test Chips & Test Structures: Various halfmicrometer process test chips and test structures shall be designed, fabricated, documented, and delivered for the purpose of providing information to the Government about the state of process development and control, detection of defects and faults, yield, and reliability. Information obtained from the periodic evaluation of the test structures shall be used to update yield and cost models and availability (Section 3.5.2). These test structures shall be designed specifically for automated wafer-probe measurement and data-interpretation procedures. Test structures shall be designed for electrical measurement, as opposed to visual or electron-optical measurement. In order to provide a uniform measurement methodology and to minimize the number of probe cards, test structures shall use the 2x10 probe-pad array (Ref. 1). The probe pads shall be on 160 micrometer centers. All 2x10 probe-pad blocks shall be oriented on the wafer with their long dimensions in the same direction (i.e: either horizontally or vertically). Five classes of test structures, as defined in the following paragraphs, shall be designed, fabricated, and evaluated.

Combinations of the test structures defined in 3.1.5.1 through 3.1.5.5 may be implemented within a mask set, limited by the minimum number of recurrences on the wafer required for a given test structure. The minimum count required shall be a function of the importance of the specific test and maturity of the process. Test structures shall be included in each wafer lot at a count commensurate with the maturity of the process.

A radiation test plan shall be submitted for approval by the Government. The plan shall provide for testing (as required by the environment in Section 4.2), reporting test results and delivery of devices for test to the Government.

3.1.5.1 Electrical-Parameter Test Structures: Structures for monitoring process and device parameters shall include as a minimum: (1) cross-bridges (Ref 2) for measurement of sheet resistances and electrical linewidths of conducting layers (Cross bridges shall be fabricated at the minimum dimensions specified by the design rules.); (2) minimum-geometry contacts for four terminal measurement of interlayer resistances of all conductor-insulator-conductor combinations specified by the design rules; (3) representative transistors of all types supported by the fabrication

process and the design rules (For MOS technologies, a suggested minimum set consists of a minimum-geometry transistor, transistors with width/length ratios of 10:1 and 1:10, and a large square transistor. For bipolar technologies an analogous set is to be defined.); (4) capacitors for measuring thickness and reliability of insulator layers;. and (5) elementary circuit functions of 100 to 5,000 gates of which at least one shall exceed 4,000 gates to indicate the producibility of initial VHSIC chips.

These test structures shall be organized as a group of 2x10 pad blocks replicated once for each chip on the wafer. Electrical parameters (including: sheet resistances, electrical linewidths, contact resistance, transistor parameters, electrical thickness of dielectric layers, contact continuity, conductor continuity, bridging, leakage current, insulator breakdown, and insulator integrity) shall be measured on the test chips and structures using wafer probe techniques. Additional test structures may be added as appropriate for a particular technology and fabrication process.

3.1.5.2 Global-Defect Test Structures: Structures for detecting and characterizing processing problems or incorrect design rules resulting from relatively uniformly-distributed defects on a wafer and that do not call for large random-fault arrays, shall be utilized. Test-structure functions shall include: (1) contact continuity; (2) conductor continuity; (3) bridging between conductors; (4) leakage current; (5) insulation breakdown; and (6) insulation integrity. They shall use the 2x10 probe-pad array. Initially, all relevant layers and layer combinations shall be included. Global defects in the process and random-defect density shall be determined by analysis of the data patterns from the above measurements. The above data shall be used to optimize the process for reliability, performance and yield. Individual layers and layer pairs may be deleted upon presentation of experimental data that justify their deletion.

3.1.5.3 Random-Defect Test Structures: Structures for estimating the density of processing defects may be either arrays of simple elements such as conductor crossovers, contacts, or circuit macros that are completely testable. Random-defect or indicator-circuit arrays shall be suitable for standard failure-analysis procedures to determine the nature of random defects. The size of random-defect structures shall be adjusted for measured yield values substantially different from zero or 100 percent, in order to track the progress of process development.

3.1.5.4 Process-Limit Test Structures: Process-limit-test structures shall be used for estimating the design margin for processing variations in the baseline process in normal operation. These shall include electrical-parameter-test structures with systematically varied dimensions for characterization of size effects, and other structures that may be appropriate for a particular process, for evaluation of variations in doping levels, deposition thicknesses, and other process parameters that may be selected for evaluation by agreement between the Contractor and the Government.

3.1.5.5 Reliability Test Structure: Reliability structures shall be used to assess effects of time-dependent stresses resulting from varying external stimuli and characterize parameter/defect stability. The

Contractor must correlate measurements on wafer-level-test structures with traditional packaged-circuit reliability measurements, and shall recommend methods for correlation. The contractor shall also perform reliability-assessment by application of electrical and environmental stresses. The results of predicted reliability shall be correlated to observe reliability after stressing.

3.1.6   Intermediate Test Vehicle: A halfmicrometer VHSIC intermediate test chip shall be designed, documented and submitted to the PCO for approval prior to release for fabrication. This test vehicle shall be a chip designed to operate as a Bus Interface Unit (BIU). (See 3.5.1). This test vehicle must have an on-chip clock speed of 100 MHz. The purpose of this chip is to validate the operation of the baseline process, with the most stringent design rules, and to verify the capability of the automated design system. Following approval of the design, this chip shall be fabricated, tested, and delivered to the government with complete documentation. The contractor shall not begin fabrication of the functional VHSIC chips (See 3.1.7, 3.3.2 and 3.4.3) until forty-five days after submission of the intermediate design test vehicle (See 3.1.6, 3.3.2 and 3.4.3) to the Government for approval or until receipt of Government approval to proceed, whichever comes first.

3.1.7   VHSIC Chip Fabrication: Following approval of the design of the intermediate test vehicle, the first full random logic custom-designed VHSIC chip shall be developed. This VHSIC chip shall be fabricated, tested and delivered to the Government for evaluation. The tests must demonstrate that the chip meets the minimum requirements of section 3.1.1 and the specific requirements of section 4.0. The performance advantages of this chip and the intermediate test vehicle chip shall be demonstrated in the brassboard module. Typical device parameters and their variations, detailed test and measurement techniques, process-control parameters, ranges and tolerance shall be established, demonstrated and documented. VHSIC chip cost shall be estimated and documented. The contractor shall not begin fabrication of the random-logic custom-designed VHSIC chip until forty-five days after submission of the design and floor plan (See 3.3.5) to the Government for approval or until receipt of Government approval to proceed, whichever comes first.

After completion of design and fabrication of this first VHSIC chip, any additional chips required for the brassboard module and major brassboard demonstration (see 3.4.1, 3.4.2, 3.4.3, 3.4.6) shall be fabricated by the same procedures.

3.1.8.   Pilot Line: A pilot production line for halfmicrometer VHSIC chips, with sufficient automation to achieve the minimum production rate necessary to satisfy contractor projected technology insertion and evaluation requirements by 1990, shall be established, documented, and demonstrated. The BIU and random logic chips shall be fabricated, tested, and delivered to validate the control and repeatibility of performance parameters, chip yield and wafer throughput. A cost model of the pilot line shall be formulated to establish the acquisition cost for the specific VHSIC halfmicrometer chips over time. (see 3.4.5)

3.1.9   Chip-Manufacturing Techniques: A procedure to satisfy DoD's production requirements for VHSIC half micrometer chips, as projected by the contractor, shall be prepared, documented and delivered. Unique equipment(s) and/or facilities required to implement this plan for full

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scale manufacturing of halfmicrometer VHSIC circuits using the processing techniques developed under section 3.1 shall be defined and specifications documented and delivered to the government. These specifications shall include requirements for computer-aided manufacturing, process control, and the equipment refinements necessary to realize cost-effective and consistant yields for VHSIC circuits in a production-line environment. A viable and effective procedure for making this standard and non-standard equipment, including standard and non-standard software interfaces, available to other DoD contractors, shall be developed, documented and delivered.

3.2 Packaging

The objective of this task is to develop and document packaging concepts, designs and hardware which shall permit half micrometer VHSIC chips to achieve their full performance, reliability and environmental capability. The packaging approach shall provide solutions to the problems of hermeticity, moisture content, thermal management, operating speed, pin-outs and interconnections, interfaces, assembly, standardization, solderability, and mechanical integrity, along with inspection and rework techniques for the package/board assemblies. Repair and rework methods shall be defined where possible for the following package types:

3.2.1 **Single-Chip Packages:** Single-chip packages and interconnect methods meeting the general requirements of section 3.2, and compatible with existing VHSIC Phase 1 packages, shall be designed, fabricated, tested, documented, and delivered. These packages shall be capable of being used in conjunction with other manufacturers' packages which may be surface or thru-hole mounted.

3.2.2 **Multi-Chip Packages:** Multi-chip packages which may be necessary to achieve cost, performance, thermal management, pin limitation, size and weight requirements of the brassboard module demonstration and the Submicrometer program shall be designed, fabricated, tested, documented, and delivered. Such packages shall be in general conformance with the objectives of section 3.2. Analysis of the single chip packaging restraints which dictate the need for multichip packages shall be provided. In addition details of the multichip package to be used shall include substrate type, method of chip-to-chip interconnect within the package and chip-to-package interconnection. Testing of multi-chip packages shall be performed from the package terminals without the need for internal probing of the package. The circuitry within the package shall be designed and demonstrated to show:

(1)   100% chip-to-chip interconnectivity has been achieved.

(2)   electrical function verification.

(3)   fault isolation to the single chip level.

All such packages developed shall be compatible with single-chip VHSIC Phase 1 packages.

3.2.3 .Board/Module Packages: Second-level. multi-layer printed circuit boards and/or multi-layer ceramic substrates shall be designed, fabricated, tested, documented, and delivered. These boards shall be used to implement the brassboard module for a laboratory demonstration of halfmicrometer VBSIC capability. Choice of the interconnect structure should consider dielectric constant minimization; match of thermal coefficient of expansion between the package board or substrate; thermal management from the 1st to the 2nd level assembly and from the module to the back plane level assembly. Tradeoffs shall be considered in the line/space geometries versus the number of layers.

3.3 Design

The objective of this task is to integrate the necessary design tools together with a capability for using the VHDL, to develop a design methodology to include testability and fault tolerance, and to design and layout the full random-logic VBSIC chips.

Chip designs which provide for continued operation under the conditions of section 4.2 shall be developed and implemented. This effort shall include appropriate modeling and simulation. Design approaches of section 3.3 shall apply. The radiation hardness shall be verified with test structures, macrocells, and intermediate test vehicles (sections 3.1.5 and 3.1.6).

3.3.1 Hierarchical Design System: An hierarchical design system shall be demonstrated, documented and used for the custom-logic, halfmicrometer VBSIC chip designs. This system shall provide a hierarchical design capability extending from the system level to the chip-pattern generation level. No new computer-aided design (CAD) tools shall be developed under this program; however, CAD tools and a VHDL shall be made available from the VBSIC IDAS program. While the use of these tools from the IDAS program is not mandatory for the proposed chip designs, it is required that the contractor host, exercise, evaluate, and support a beta test site for the tools available under the IDAS 1/2 program. It is required that the VHDL be incorporated into the contractor's system, at least through the use of translators, in order to provide a VHDL description of all chips developed.

3.3.1.1 VBSIC Hardware Description Language (VHDL): A VHDL description of all chips and their interfaces shall be developed and delivered. The description shall provide detailed definition of chip primitives, functional processing modules, macrocells or similar partitions which are used in the design process. In addition, all chips shall be simulated with the VHDL simulator.

3.3.1.2 Support Software: Support Software. including higher order language (HOL) software development systems, which facilitate cost-effective programming of the VBSIC chips and brassboard module shall be developed and delivered. Ada shall be used as the HOL. Off-chip compilers may be used as appropriate.

3.3.2 Design Simulation and Verification: A hierarchical design simulation shall be performed to verify the designs through all levels of the design process in an effort to achieve one pass chip design

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and fabrication. Simulation capability shall be compatible with the speed,
complexity, and design-performance parameters of the halfmicrometer circuits
with clearly defined interfaces between simulation levels. The simulation
shall include models, model parameters, process and device characteristics,
which are required for cost-effective simulation of process, device, cell
library (primitive), logic, register transfer, and subsystem functional
levels. The simulation approach shall be capable of modeling the operation
of brassboard module subsystems which contains a number of chips. The
techniques applied must demonstrate the feasibility of providing accurate
floorplanning and timing analysis at all levels (chip, board and system) as
well as chip boundary simulation. (sections 3.1.6, 3.1.7, 3.4.1, 3.4.2, and
3.4.3)

3.3.3   Design Methodology: Design techniques shall be
developed, documented, and demonstrated which provide increased testability
and reliability of chip performance through the inclusion of on-chip testing
and fault-tolerant designs. The design approach shall be such that
interface levels and supply-voltage requirements are consistent with
interoperability of all VESIC halfmicrometer chip sets (see 3.5.1).
User-design support systems selected from existing design methodology and
design tools must be compatible with the chip-architectural approach
selected.

3.3.4   Testability: A design approach shall be adopted and
documented that provides for built-in-test at the chip and module levels,
facilitates the capability to functionally exercise the chip, and fully
verifies the logic integrity of the chips from an external source. The chip
area to be utilized for an adequate test and fault-detection and/or
fault-isolation capability and fault detection/isolation requirements and
shall be consistent with the chip functional complexity and shall be
provided as a part of the overall design details provided for government
approval. (sections 3.1.6, 3.1.7, 3.4.1, 3.4.2, 3.4.3 and 3.5.1)

3.3.4.1   Built-in-Test Fault Detection And Fault Isolation: Any
design concepts selected for built-in-test and fault isolation must reflect
approaches which make optimum use of on-chip and system-level built-in-test
capability. Fault-tolerant designs and concurrent fault monitors must be
included and documented in the design approaches proposed for
implementation. An analysis and evaluation of the fabrication, performance,
complexity, and cost tradeoffs which result from providing the built-in-test
and fault isolation capability, shall be conducted for all design approaches
considered. The built-in-test and fault isolation capability shall be such
that as a minimum fault isolation is achievable to the lowest replaceable
level of the system.

3.3.4.2   Built-in-Test Fault Coverage: The built-in test
function shall achieve and demonstrate at least 95% coverage at the chip
level of single stuck-at faults for halfmicrometer chips as determined by a
digital fault simulator. The figure for test coverage shall be given in
meaningful terms, i.e: "95% of equivalent fault classes". For CMOS
halfmicrometer built-in test, at least 75% coverage of stuck-open faults, as
verified by statistical analysis, shall be achieved and demonstrated.

3.3.5   Chip Design and Layout The architectural approach defined
in section 3.4.2 shall be instantiated where halfmicrometer chip
requirements are identified using the hierarchical design system and design

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methodology described in this section (3.3). The contractor shall design and document chips required to implement the specific brassboard module, and any optional major brassboards exercised. Chip documentation shall include complete functional, electrical programming and testing specifications, a VHDL description , and an application guide. Detailed definitions of chip primitives, functional processing modules, macrocells or similar partitions which are used in the design process shall be provided. Chip design/architecture shall include design testability. New and/or improved design architectural concepts, standard interfaces and conventions shall be developed to minimize the number of custom circuits for signal processing applications, in addition to reducing the costs of whatever remaining customization shall be required for additional applications.

3.4   Applications

The objective of this task is to design, fabricate and test a brassboard module in order to demonstrate the advantage of the VHSIC halfmicrometer technology.

3.4.1   Major Brassboard Technology Insertion: The contractor shall implement the proposed applications to take advantage of the architecture and halfmicrometer chips defined under the task of section 3.4.2. Advantages shall be identified clearly stating that the chosen brassboard system requires halfmicrometer VHSIC performance.

This task, when exercised, is to complete a full subsystem processor implemented in VHSIC halfmicrometer technology and ready for technology insertion into a specific weapon system. This shall include the design, simulation, fabrication, testing and documentation of all required VHSIC halfmicrometer chips and all required additional modules for a major brassboard subsystem prototype.

3.4.2   Chip Definition and Brassboard Module Architecture: The contractor analyses shall identify systems' requirements of the 1990's which can benefit most from VHSIC halfmicrometer technology. These systems shall be partitioned into a viable architecture of standard modules for implementation in VHSIC halfmicrometer chips. All halfmicrometer chips required to support these modules shall be defined. One module from this set of modules, which can be applied to a number of specific systems, and the halfmicrometer chip(s) required to populate it, shall be selected by the Government as a laboratory brassboard demonstration of the advantages of halfmicrometer technology. A system/subsystem maintainability concept and test methodology shall be defined and incorporated into the brassboard module design. An analysis of the algorithms to be implemented, hardware/software tradeoffs, functional commonality, I/O requirements, EOL (Ada) software programming requirements, memory requirements, and functional-throughput requirements shall be performed. This module should be implementable with one or more chips of a random-logic, custom-designed halfmicrometer VHSIC chip type, plus a bus interface unit (BIU) which is implemented in a VHSIC halfmicrometer chip and Phase 1 VHSIC chips or other commercially available ICs where appropriate. Detailed designs of the full brassboard module including hardware, operating software, and applications software shall be documented and delivered to the Government. The

contractor shall not begin fabrication of the brassboard module until forty-five days after submission of the feasibility of all chip designs and simulation and brassboard module designs and simulations (See 3.4.2, 3.1.6, 3.1.7, 3.3.2 and 3.3.4) to the Government for approval or until receipt of Government approval to proceed, whichever comes first.

3.4.3 VHSIC Chip Design: Design and document the set of at least one random-logic, custom VHSIC chip required to implement the brassboard module demonstration defined in section 3.4.2. A chip design architecture shall include design for testability as specified in section 3.3.4 and for functional performance requirements developed to satisfy the design and fabrication of the brassboard module. Chip documentation shall include complete functional, electrical, programming, test specifications, VHDL coding of the VHSIC chip(s) and their interfaces, and an application guide. The design cells required to implement these VHSIC chips shall be determined, documented and delivered to the Government. (see 3.1.7)

3.4.4 Software Development: System support software shall be selected, developed, documented, delivered, and structured such that a user programmer can effectively program, debug, validate, evaluate, and implement the functional algorithms in the halfmicrometer VHSIC chip architectural approach chosen. In addition, the software shall support the overall failure management and test concept. The VHSIC Phase 2 halfmicrometer chips must be programmable in Ada.

3.4.5 Life Cycle Cost Factors: Life cycle cost factors shall be identified for use of VHSIC technology in system design, including materials, processing, yield, testing, packaging, fault diagnostics, maintainability, reliability and logistics.

3.4.6 Brassboard Module Fabrication: A brassboard module, utilizing halfmicrometer VHSIC chips, shall be designed, developed, functionally programmed, tested, documented, and delivered. The performance and test results, including environmental conditions, shall be documented and reported. The demonstration shall be conducted in a laboratory environment with electrical-input data, output processing and display supplies from outside the module, representative of the system(s) processing/data handling requirements. The brassboard module is expected to make use of and demonstrate the maximum performance capability of the halfmicrometer VHSIC chips. This brassboard module shall be a functional partition of the brassboard identified in section 3.4.1.

3.5 Technology Transfer/Business Strategy

3.5.1 Interoperability Standards: Interface/interoperability standards shall be established by agreement among all VHSIC Phase 2 Submicrometer contractors and the Government COTR's to assure that all chips developed under the VHSIC Phase 2 Submicrometer program are interoperable, both electrically and physically. Standard voltage level(s) shall be established and utilized for all chips and input/output levels shall be equivalent for all chip interfaces, whether contained in a single or multi-chip package. A VHSIC halfmicrometer Bus Interface Unit (BIU) chip shall be developed to facilitate module interoperability with a standard

interconnect system bus. The BIU and any other VHSIC chips developed under this Phase 2 VHSIC Submicrometer program shall interface directly to a standard system maintenance bus to be defined by agreement among all the VHSIC Phase 2 Submicrometer contractors and the Government COTR's. All these standards shall be documented and delivered.

3.5.2 <u>Availability</u>: A procedure shall be developed and documented for making halfmicrometer VHSIC chips, chip boundary simulations, and brassboard modules available to other DoD contractors and Government laboratories in a timely and affordable manner. Methods for establishing price, delivery schedule, availability from second source(s) and limitations shall be defined. Describe procedures for providing both processing and design/architecture services, clearly defining the interfaces and input requirements, and second sourcing. Methods for supporting gate-array personalizations and other modifications to basic designs shall also be described.

3.5.3 <u>Second-Source</u>: A second source plan shall be developed which describes the transfer of processes and techniques for chip fabrication utilized in the basic program, and to provide chips with significant yield. The second source plan shall cover process techniques in sufficient detail to insure that if a second source were to be established, VHSIC chips meeting the same functional and packaging specifications achieved by the prime source could be delivered. Procedures for making parts available, a schedule and any limitations shall be documented and delivered.

3.5.4 <u>External Demonstration</u>: The purpose of this task is to define, establish and demonstrate a design interface to utilize the VHSIC chip designs and fabrication capabilities developed under this program. This demonstration shall address the requirements of non-VHSIC DoD contractors for technology insertion of new submicrometer VHSIC chips. The contractor shall be provided a VHDL description and all necessary supporting documentation needed to fabricate a chip designed by a non-VHSIC system contractor. All software and test vectors for wafer probe testing of this chip shall be provided by the system contractor to the VHSIC contractor who shall perform the wafer probe tests. Packaged VHSIC chips shall be delivered to the system contractor for final test and evaluation.

4.0 ENVIRONMENTAL, RELIABILITY AND TESTABILITY REQUIREMENTS

VHSICs developed during this program shall be required to meet the following specifications which are the minimum to meet the broad range of DOD system applications. If a system application is selected that has requirements in excess of these minimums, the system environment requirements shall be met.

4.1 <u>Temperature Range</u>

Operate over the full military temperature range of an ambient -55°C to a +125°C while concurrently meeting the minimum nuclear requirements.

4.2 <u>Trade-off Radiation Requirements</u>: VHSIC's developed shall be required to meet one of the following specifications for the process chosen:

4.2.1 Baseline Radiation Requirements

4.2.1.1 Integrated Radiation

Operate without radiation induced failures in a radiation environment of at least 5×10^4 rads (Si), 2×10^5 rads (Si) goal at a rate of 50-200 rads (Si)/sec.

4.2.1.2 Transient Radiation

Operate (survive) without radiation induced permanent failures after a transient radiation dose during operation of 10^{10} rads (Si)/sec for 30 nanosecond pulse, with a goal of 10^{12} rads (Si)/sec for 30 nanosecond pulse.

4.2.1.3 Transient Upset

Operate without transient upset through a radiation pulse of 1×10^8 rads (Si)/sec, goal of 10^{10} rads (Si)/sec for 100 nanosecond pulse.

4.2.1.4 Neutron Damage

Operate without permanent damage after a neutron radiation dose during operation of at least 5×10^{12} neutrons/cm^2, 1MeV equivalent.

4.2.1.5 Single Event Upset (SEU)

A goal of less than 1×10^{-10} errors/bit/day in the 10 percent worst case geosynchronous orbit presented in reference 3 and be latch up free.

4.2.2 Enhanced Radiation Requirements

4.2.2.1 Integrated Radiation

Operate without radiation induced failure in a radiation environment of at least 2×10^5 rad(Si), with a goal of 1×10^6 rad(si) at a rate of 50-200 rad(Si)/sec.

4.2.2.2 Transient Radiation

Operate (survive) without radiation induced permanent failure after a transient dose during operation of 10^{10} rad(Si)/sec for 30 nesc pulse, with a goal of 10^{12} rads(Si)/sec.

4.2.2.3 Transient Upset

Operate without upset through transient radiation pulse of 10^8 rad(Si)/sec for 100 nesc radiation pulse, with a goal of 10^{10} rads(Si)/sec.

4.2.2.4 Transient Induced Latch-up

Operate without transient radiation induced latch-up following a radiation pulse of 10^9 rad(Si)/sec for a 100 nsec pulse, with a goal of 10^{11} rad(Si)/sec.

4.2.2.5 Neutron Damage

Operate without permanent damage after a neutron fluence of 5×10^{12} neutron/cm^2 (1MeV equivalent) with a goal of 10^{14} neutron/cm^2.

4.2.2.6 Single Event Upset (SEU)

Operate with single event upset-rates of less than 1×10^{-10} errors/bit/day for memory (requirement) and 1×10^{-10} errors/gate/day (goal) for logic circuits in the particle flux of the 10 percent worst case environment in geosynchronous orbit presented in reference 3.

4.3 Failure Rates

Delivered, packaged chips suitable for testing shall have failure rates, after screening and burn-in not exceeding .006% per 1000 hours at 60% confidence level both while operating and while stored over the range -55°C to 125°C ambient temperature. Reliability and qualification demonstration test plans that detail test procedures to demonstrate the reliability of the halfmicrometer VHSIC chips shall be prepared and submitted for Government PCO for approval.

4.4 Electromagnetic Pulse & Electrostatic Discharge

Delivered brassboard modules require the following protection against electromagnetic pulses and electrostatic discharge: (1) Risetime - 0.27 microsecond; (2) Pulse width - 7.1 microsecond; (3) Fall time - 7.1 microsecond; (4) Amplitude - 500 volts, either polarity; and (5) Voltage source impedance - 100 ohms.

4.5 Multi-Chip Carrier Testing

Multi-chip carrier testing shall demonstrate 100% I/O chip-to-chip testing and pass functional verification testing.

4.6 Module Packaging

A brassboard module packaging shall be developed based on ongoing Service standardization efforts.

4.7 Military Standards

All chips and packages in section 3.2 must have the basic capability of being qualified for use as a MIL-M-38510, MIL-STD-883, Class B device, (i.e: organic adhesives of only the highest quality; lead

type and substrate type, meet true system shock, vibration, thermal cycle, thermal shock, etc.) Environmental and reliability testing and failure analyses shall be performed to provide an indication that packaged VHSIC chips can satisfy the requirements and goals of Sections 3.0 /4.0.

5.0 GLOSSARY

5.1 VHSIC

Acronym for "Very High Speed Integrated Circuits." This acronym was developed to describe the program to develop very large scale integrated circuits applicable to DoD needs, particularly very high speed signal processing. The speed-density product figure-of-merit requirement is 1×10^{13} gate-Hz/cm. The acronym is also used to describe the integrated circuits that shall be developed under the program.

5.2 Phase 0

Refers to the program part called "Program Definition" to provide a plan and approach for Phase 1 and 2.

5.3 Phase 1

Refers to the parts of the program during which electronic brassboard subsystems are constructed using VHSICs based on 1.25 micrometer minimum feature sizes (Phase 1a), and in which development work is carried out to achieve VHSICs based on submicrometer feature sizes (Phase 1b).

5.4 Phase 2

Refers to the program parts oriented as follows:

5.4.1 Technology Insertion of Phase 1: A part of the program which addresses military subsystem/system feasibility studies and demonstration of the VHSIC Phase I chip set in actual weapon systems.

5.4.2 Integrated Design Automation System (IDAS): A part of the program which shall identify, enhance and integrate computer-aided tools to provide an automated design capability. An environment to assist in system design trade-off decisions, design capture and specification analysis/synthesis shall be developed.

5.4.3 Submicrometer Technology Development: The part of the program which shall provide a capability for further major improvements in system performance and reliability. Extensions of the state-of-the-art in VHSIC design, architecture, fabrication, software and test capabilities to halfmicrometer minimum feature size shall be developed.

5.5 Phase 3

Technology efforts which are generic in nature and supportive of Phase 1 and 2.

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5.6   VHSIC Architectures

A structure by which VHSIC devices are interconnected, addressed and programmed to meet design objectives of application algorithms. This definition includes interconnection or bussing, instruction set, special functions, control, addressing I/O schemes made compatible with one operating system including executive and language programming issues. Interconnection of VHSIC devices shall produce a machine which can be used to perform many signal processing as well as generic logic and arithmetic functions.

5.7   Subsystems

This refers to an assembly of ICs and related components such as a signal/data processor to . performs a function which can be incorporated into an entire weapon system such as an aircraft, missile, tank, or ship.

5.8   System Demonstration

This refers to the validation and testing of an electronic subsystem in a system test bed.

5.9 . Subsystem Brassboard

An operating assembly for evaluation purposes with proper input and output terminals, containing ICs and other components (as required) all assembled, interconnected and packaged.

5.10   Functional Throughput Rate FTR

Functional Throughput Rate is the product of on-chip clocking speed in Hz and the gate density in gates per square cm.

5.11   Chip

A single monolithic silicon integrated circuit.

5.12   Automated Pilot Line

A facility consisting of equipment and personnel which is capable of fabricating, packaging, and testing VHSIC chips on a sustained basis. It employs computer-aided manufacturing (CAM) techniques and automatic controls necessary to assure repeatability and consistent yield.

5.13   VHSIC Hardware Description Language (VHDL)

VHSIC Hardware Descriptive Language. VHDL is a modern hardware description language for use in describing VHSIC chips and to expeditiously incorporate VHSIC chips into systems.

5.14   VHSIC Halfmicrometer Technology

VHSIC chips with physical dimensions of 0.5 micrometer for the minimum feature size. Minimum feature size is defined as the smallest lateral dimension, achieved through lithography or directed beam techniques, which affects device/circuit performance.

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5.15 Brassboard Module

An operating subassembly of a brassboard.

6.0 REFERENCES:

1. M.G. Buehler, "Comprehensive Test Patterns with Modular Test
Structures: The 2xN Probe Pad Approach," Solid State Technology, volume 22,
pp 89-94 October 1979.

2. M.G. Buehler, S.D. Grant, W.R. Thurber, "Bridge and van der Pauw
Sheet Resistor for Determining Line Width of Conducting Layers," Journal of
Electrochemical Society, volume 125 pp 650-654 1978.

3. E.L. Petersen, P. Shapiro, J.H. Adams, Jr., and E.A. Burke,
"Calculation of Cosmic-Ray Induced Soft Upsets and Scaling in VLSI Devices,
IEEE Trans. Nucl. Sci., NS-29, No. 6, December 1982.

GLOSSARY OF ACRONYMS AND TECHNICAL TERMS

4PM	Four Port Memory
A-6F	Navy Attack Aircraft
AASP	Advanced Anti-Radiation Missile Signal Processor
ABBM	Acoustic Beamformer Brassboard Module
ACE	Array Computing Element
ACS	Array Controller/Sequencer
ADB	Advanced Digital Bipolar (Honeywell technology)
AEBLE	Advanced Electron Beam Lithography Equipment
AEGIS	Advanced Electronic Guidance and Intercept System
AFIT	Air Force Institute of Technology
AG	Address Generator
AI	Artificial Intelligence
AJ	Anti-Jam or Jam Resistant
ALU	Arithmetic Logic Unit
ALWT	Advanced Lightweight Torpedo (MK-50)
AMAC	Add Multiply Accumulate
AMGS	Automatic Microcode Generation System
AMSDS	Automated Microcode Compiler Synthesis & Design System
AMTE	Automated Microcircuit Test Equipment
AN/ALQ-131	Airborne Pod-Mounted Electronic Countermeasure (ECM)
AN/ALR-56C,74	AF Radars
AN/APG-65	Navy Coherent Multimode Pulse Doppler Radar
AN/APG-68	Airborne Fire Control Radar
AN/AYK-14(V)	Navy Embedded Standard Airborne Computer
AN/BQQ-5	Sonar System
AN/TPQ-36,37	Army Radars (Firefinder)
AN/UYS-1,2	Navy Standard Signal Processors
AOSP	Advanced Onboard Signal Processor
AP	Arithmetic Processor
APC	Array Processor Controller
APE	Asynchronous Processing Element
APIO	Array Processor Input/Output
APU	Arithmetic Pipeline Unit; Array Processing Unit
ARM	Anti-Radiation Missile
ASP	Advanced Signal Processor
ASW	Antisubmarine Warfare
ATE	Automatic Test Equipment
ATF	Advanced Tactical Fighter
ATR	Auto Target Recognition
AU	Arithmetic Unit
AV-8B	Marine Vertical Takeoff and Landing (VTOL) Aircraft
AWACS	Airborne Warning and Control System
AWIS	Advanced Wafer Imaging System

Ada	DoD High Order Programming Language
BEOL	Back End of Line
BIST	Built-In Self Test
BIT	Built-In Test
BIU	Bus Interface Unit
Brassboard	Field Demonstrable Electronic Model
Breadboard	Laboratory Demonstrable Electronic Model
C3I	Command, Control, Communications, and Intelligence
CAD	Computer Aided Design
CALMA	Graphics design system marketed by CALMA Corporation
CAM	Content Addressable Memory
CAM	Computer-Assisted Manufacturing
CAVP	Complex Arithmetic Vector Processor
CC-BUS	Chip to Chip Bus
CDP	Configurable Data Path (chip)
CDR	Critical Design Review
CDRL	Contract Data Requirements List
CGA	Configurable Gate Array
CMAC	Complex Multiply Accumulate
CML	Current Mode Logic
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CS	Convolver Superchip
CSP	Common Signal Processor
CSR	Configurable Static RAM
CTTC	Circuit Technology Test Chip (Honeywell)
DAST	Design, Architecture, Software, and Test
DESC	Defense Electronics Supply Center
DIFAR	Directional Frequency Analysis and Recording
DIU	Device Interface Unit
DNA	Defense Nuclear Agency
DOD	Department of Defense
DPU	Data Processor Unit
DRAM	Dynamic RAM
DSPE	Double Solid Phase Epitaxy
DTIC	Defense Technical Information Center
E-2C	Navy Airborne Warning and Control System (AWACS)
E-3A	SENTRY Air Force AWACS
E-BEAM	Electron-Beam
EA-6B	Navy EW Aircraft
EAR	Export Administration Regulations
EAU	Extended Arithmetic Unit
EAUM	Extended Arithmetic Unit Multiplier
EBL	Electron Beam Lithographic (Machine)
ECCM	Electronic Counter Countermeasures
ECM	Electronic Countermeasure
EEPROM	Electrically Erasable Programmable Read-Only Memory
EHF	Extremely High Frequency
EIS	Engineering Information System
ELINT	Electronic Intelligence

EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
EMP	Electomagnetic Pulse; Electomagnetic Potential
EMSP	Enhanced Modular Signal Processor
EO	Electro-Optic
EOSP	Electro-Optic Signal Processor
EOSPC	Electro-Optic Signal Processor Controller
EP-3E	Electronic Surveillance Aircraft
EPLRS	Enhanced Position Location and Recording System
EPUU	Enhanced PLRS User Unit
ESD	Electrostatic Discharge
ESD	Elecrostatic Discharge
ESM	Electronic Support Measure
ETM-Bus	Element Test and Maintenance Bus
EW	Electronic Warfare
F-14D	Navy Fighter Aircraft
F/A-18	Navy Fighter Attack Aircraft
FAR	Federal Acquisition Regulation
FEOL	Front End of Line
FFT	Fast Fourier Transform
FLIR	Forward Looking Infrared
FOG-11	Missile
FPAP	Floating Point Arithmetic Processor
FTR	Functional Throughput Rate
Firefinder	Army Target Locator System
GBU	General Buffer Unit
GFE	Government Furnished Equipment
GOMAC	Government Microelectronics Applications Conference
GPC	General Purpose Computer
GVSC	Generic VHSIC Spaceborne Computer
HDL	Hardware Description Language
HF	High Frequency
HOL	Higher Order Language
HSL	Hierarchical System Language
Hellfire	Anti-Armor Weapon System
Hercules	Hughes CAD system
I/O	Input/Output
IAC	Information Analysis Center
IAPU	Image Array Processing Unit
IC	Integrated Circuit
ICNIA	Integrated Communication, Navigation, and Identification Avionics
IDAS	Integrated Design Automation System
IEEE	Institute of Electrical and Electronics Engineers
INEWS	Integrated Electronic Warfare System
IPS	Instructions Per Second
IRHVTA	Infra-Red (seeker for) High Value Target Acquisition
IRST	Infrared Search and Track
ISA	Instruction Set Architecture; Imaging Sensor Autoprocessor
ITAR	International Traffic in Arms Regulations

IV&V	Independent Validation and Verification
IVTM	Interconnect Verification Test Module
IVV	Independent Validation and Verification
JTIDS	Joint Tactical Information Distribution System
LAMPS	Light Airborne Multipurpose System
LCCC	Leadless Ceramic Chip Carrier
LHX	Light Helicopter Experimental
LOFAR	Low Frequency Analysis and Recording
LP	Laser Pantography
LRE	Logistics Retrofit Engineering Program
LRM	Line Replaceable Module
LSI	Large Scale Integration
M2F2	Multimode Fire and Forget Missile
MAC	Multiplier/Accumulator
MADS	Maintenance And Diagnostics System
MC	Micro-Controller
MCP	Multichip Package
MEDFLI	Minitarized Electronic Direction Finding Location Indicator
MICROMETER	Micron = 10(-6) Meter
MICRON	Micrometer = 10(-6) Meter
MIL-STD	Military Standard
MILSTAR	EHF Satellite Communication System
MIPS	Million Instructions Per Second
MK-50	Advanced Light Weight Torpedo (ALWT)
MMG	Multimode Guidance
MMS	Mass Memory Superchip
MMW	Millimeter Wave
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MPS	Multipath Switch
MRSR	Multirole Survivable Radar
MS	Matrix Switch
MSI	Medium Scale Integration
MTBF	Mean-Time-Between-Failure; Mean-Time-Between-Fault
MTTR	Mean Time to Repair
NMOS	N-Channel Metal-Oxide Semiconductor
OPS	Operations per Second
OSD	Office of the Secretary of Defense
OUSDR&E	Office of the Under Secretary of Defense for Research and Engineering
P3	Naval Patrol Aircraft
P3-C	Navy ASW Aircraft
P3I	Preplanned Product Improvement
PAVE SPRINTER	Modular Avionics Demonstration Program
PE	Processing Element
PGA	Pin Grid Array
PI-BUS	Parallel Interface Bus (designed during VHSIC-2)
PJH	PLRS/JTIDS Hybrid
PLA	Programmable Logic Array
PLAU	Pipeline Arithmetic Unit

PLRS	Position Locating and Reporting System
POC	Proof of Concept
PPP	Parallel Pipeline Processor
PROM	Programmable Read-Only Memory
PSP	Programmable Signal Processor
PWB	Printed Wiring Board
QPL	Qualified Products List
RALU	Register Arithmetic Logic Unit
RAM	Random Access Memory
ROM	Read Only Memory
RPV	Remotely Piloted Vehicle
RTL	Register Transfer Language
RWR	Radar Warning Receiver
S3	Naval Early Warning Aircraft (including radar system)
SCM	Single-Chip Module (used interchangeably with SCP)
SCP	Single-Chip Package (used interchangeably with SCM)
SDI	Strategic Defense Initiative
SECDED	Single Error Correct, Double Error Detect
SEM	Standard Electronic Module
SEU	Speech Enhancement Unit
SEU	Single-Event Upset
SGEMP	System Generated Electromagnetic Pulse
SH-60B	(Sikorsky) Helicopter Aircraft
SI Chip	System Interface Chip (BIU + FIU)
SOW	Statement of Work
SP	Signal Processor
SPE	Signal Processing Element
SPEAR	Solid Phase Epitaxy and Regrowth
SPICE	Public Domain Integrated Circuit Simulation Program
SPS	Systolic Processing Superchip
SRAM	Static RAM; Short Range Attack Missile
SSI	Small Scale Integration
STL	Schottky Transistor Logic
STS	Signal Tracking Subsystem
SubACS	Submarine Advanced Combat System
TAB	Tape Automated Bonding
TAM	Threat Assocation Module
TISSS	Tester Independent Support Software System
TM-BUS	Test and Maintenance Bus
TOW	Tube Launched, Optically Tracked, Wire Guided Missile
TREE	Transient Radiation Effects in Electronics
TTL	Transistor-Transistor Logic
VAG	Vector Address Generator
VALU	Vector Arithmetic/Logic Unit
VBIU	VHSIC Bus Interface Unit
VCB	VHSIC Communications Brassboard
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuits
VID	VHSIC Insertion Demonstration for the EMSP
VLM	Very Large Memory

VLSI	Very Large Scale Integration
VPC	Vector Product Calculator
VPO	(DoD) VHSIC Program Office
VPSP	VHSIC Programmable Signal Processor
VSC	VHSIC Signal Conditioner
VTCA	VHSIC Transmit Control Assembly
WAM	Window Addressable Memory
WCL	Wireless Command Link
WSI	Wafer Scale Integration
XSAR	X-ray Step and Repeat Lithographic Machine
YE	Yield Enhancement
YVR	Yield Verification Run